

PG161-A00

TU106 6GB GDDR6, 192b, X16
DVI-D/DP + DP + HDMI

TABLE OF CONTENTS

Page Description

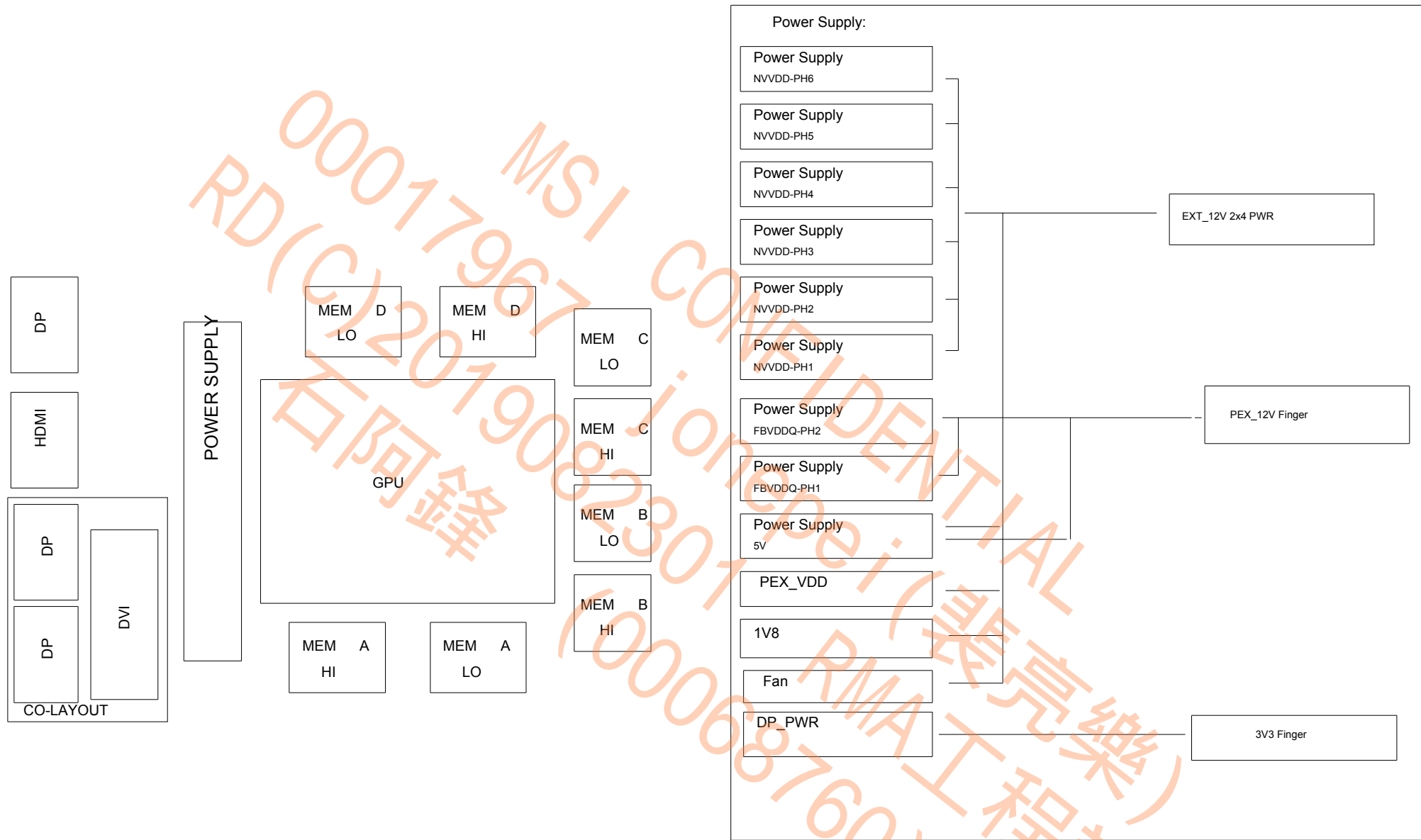
1	Table of Contents
2	Block Diagram
3	PCI Express
4	PCIe RC TERM
5	MEMORY: GPU FB_AB
6	MEMORY: FBA[31:0]
7	MEMORY: FBA[63:32]
8	MEMORY: FBB[31:0]
9	MEMORY: FBB[63:32]
10	MEMORY: GPU FB_CD
11	MEMORY: FBC[31:0]
12	MEMORY: FBC[63:32]
13	MEMORY: FBD[31:0]
14	MEMORY: FBD[63:32]
15	GPU PWR & GND
16	GPU Decoupling
17	GPU Decoupling2
18	IO: IFPAB DVI-D-DL
19	IO: IFPA DP
20	IO: IFPB DP
21	IO: IFPE & IFPF USBC NC
22	IO: IFPC HDMI
23	IO: IFPD DP
24	IO: NVHS Interface and Frame Lock
25	MISC1: Thermal, JTAG, GPIO,STEREO

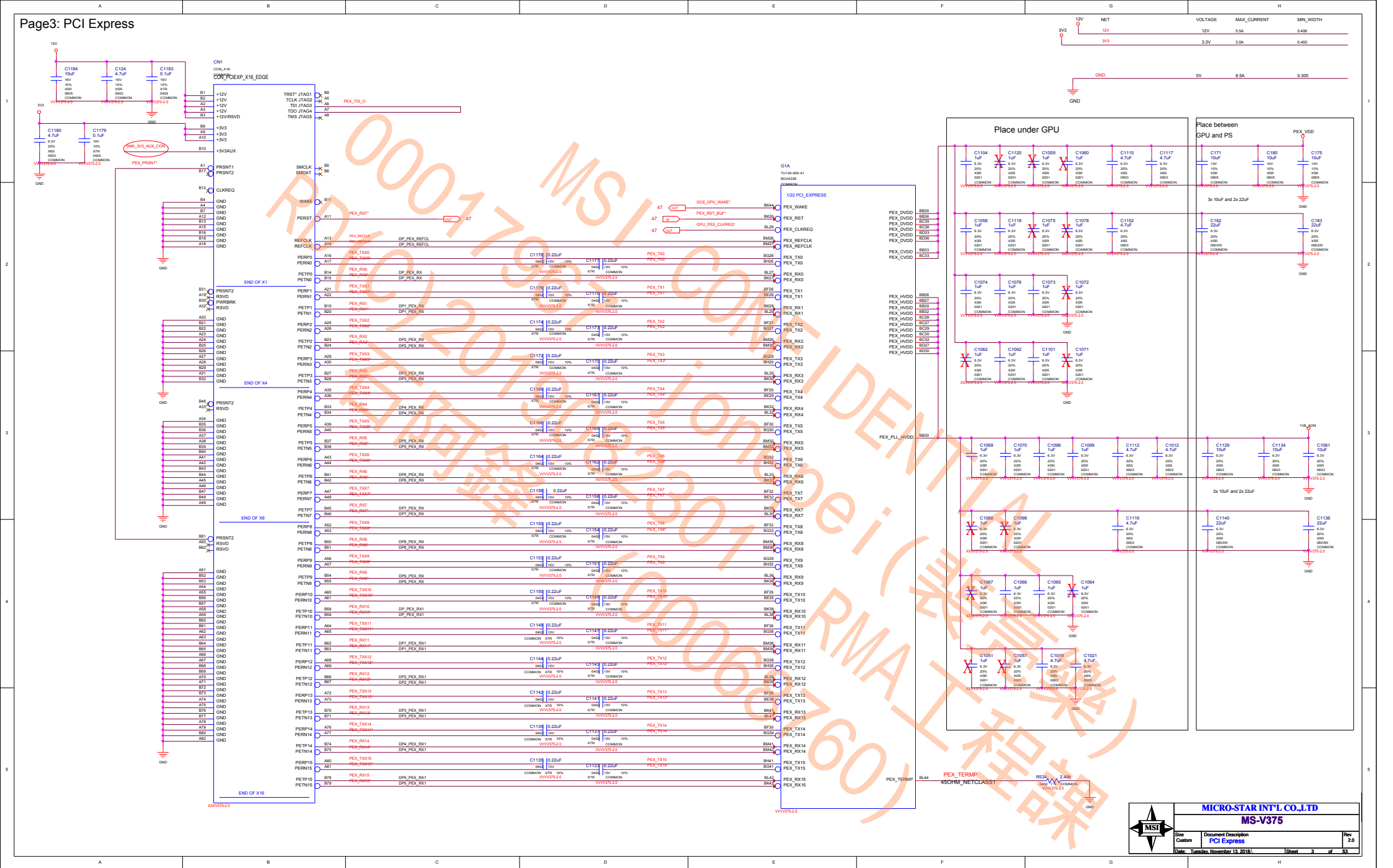
Page Description

26	MISC2: ROM, XTAL, STRAPS
27	PS: 1V8_AON
28	PS: 5V
29	PS: PEXVDD
30	PS: FBVDDQ
31	PS: FBVDDQ PH2
32	PS: NVVDD Controller
33	PS: NVVDD Controller OVR3i
34	PS: NVVDD Phase 6,4
35	PS: NVVDD Phase 3,5
36	PS: NVVDD Phase 2,1
37	PS: Input Power Balancing Switcher
38	PS: Input, Filtering, and Monitoring
39	PS: STEERING, UPB & HOT-UNPLUG
40	PS: Type-C BuckBoost
41	PD PPC
42	PS: 12V & 3V3_A SWITCHER
43	SEQ: 5V, 1V8, NV3V3 ENABLE
44	SEQ: NV, PEX, FB ENABLE
45	SEQ: VOLTAGE MONITOR
46	SEQ: DISCHARGE
47	SEQ: MISC
48	LOGO LED
49	LED DRIVER & BOOST
50	FAN

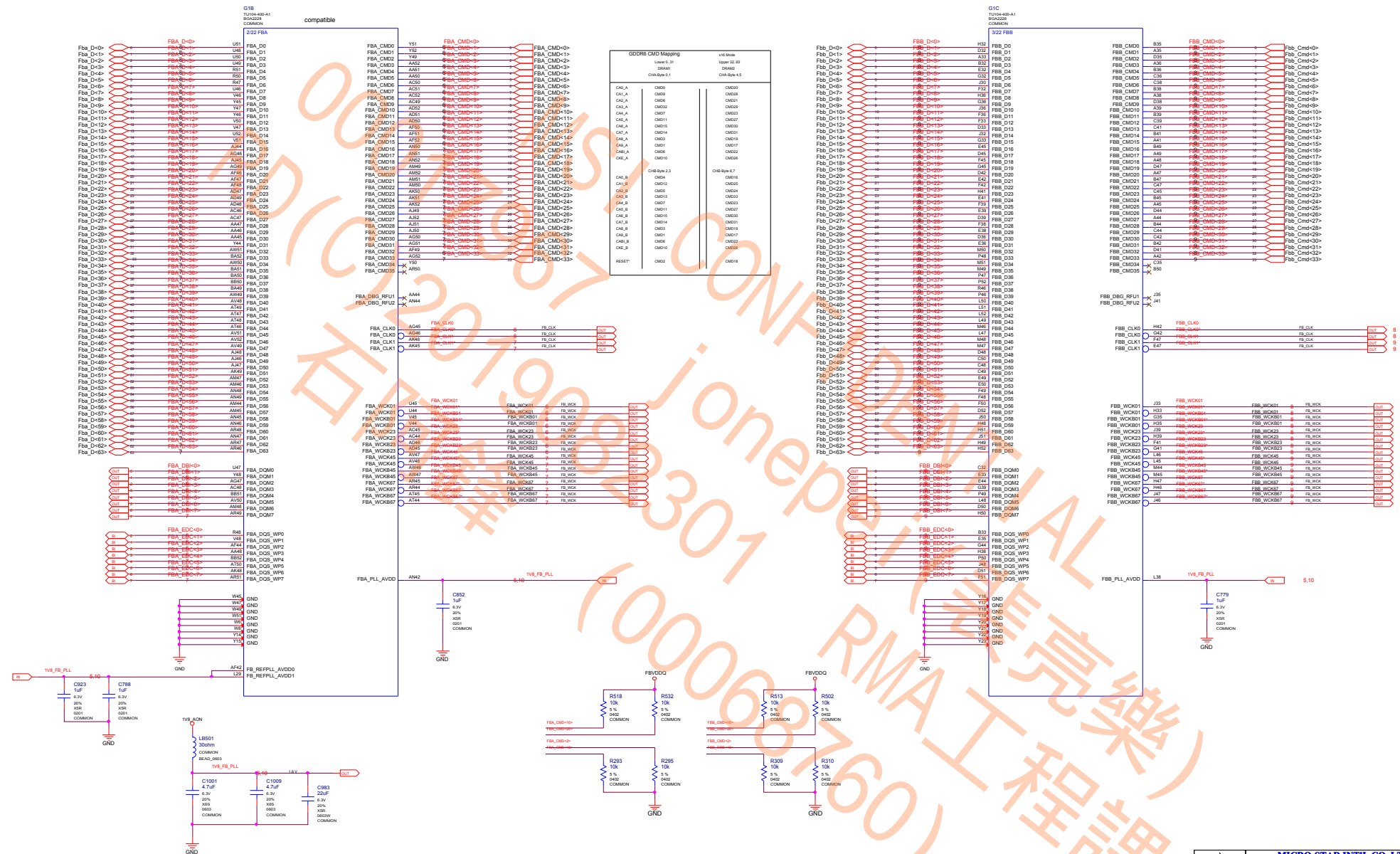
Page Description

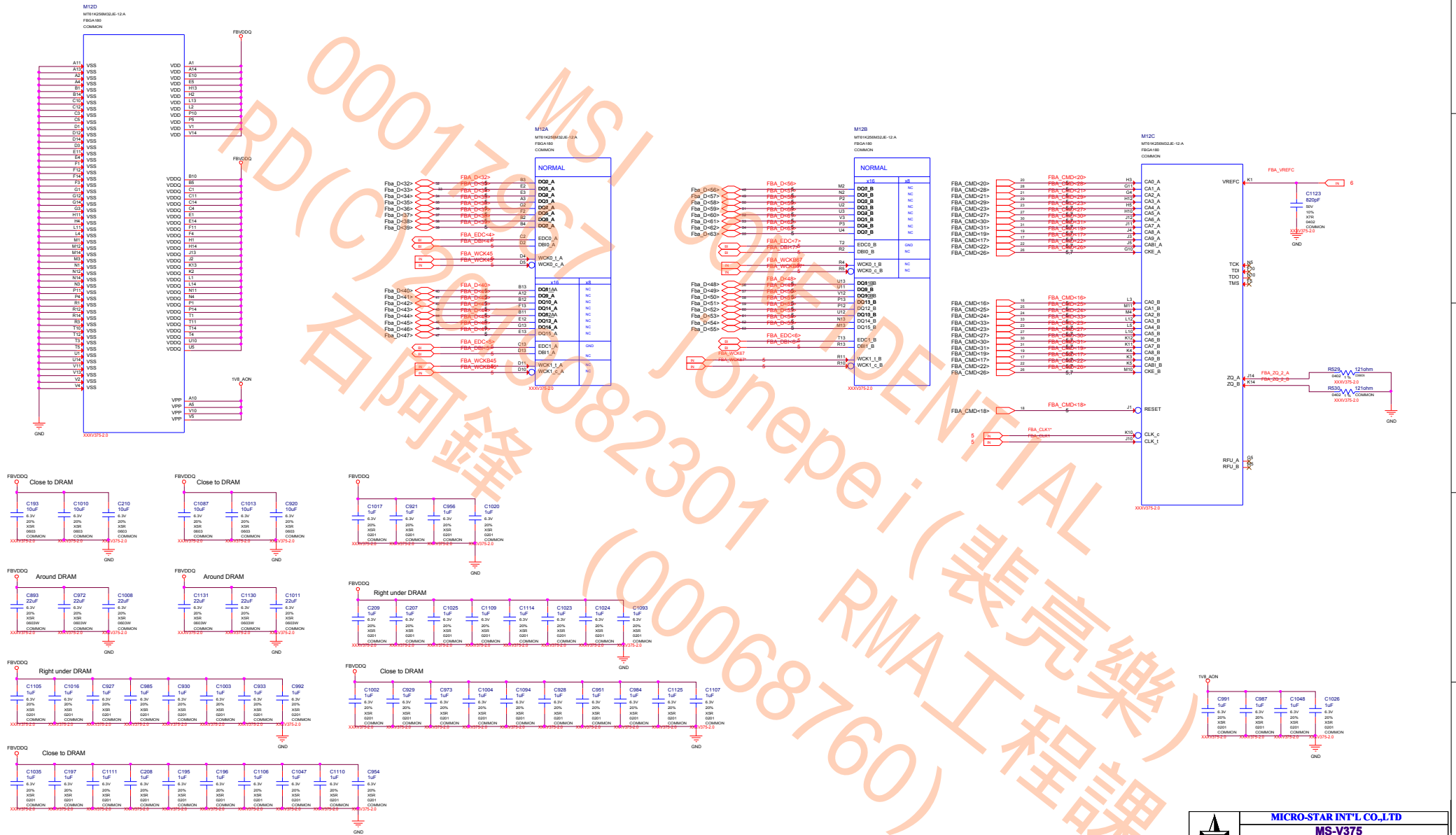
51	PS: Pre-filter
52	MECH
53	PTC

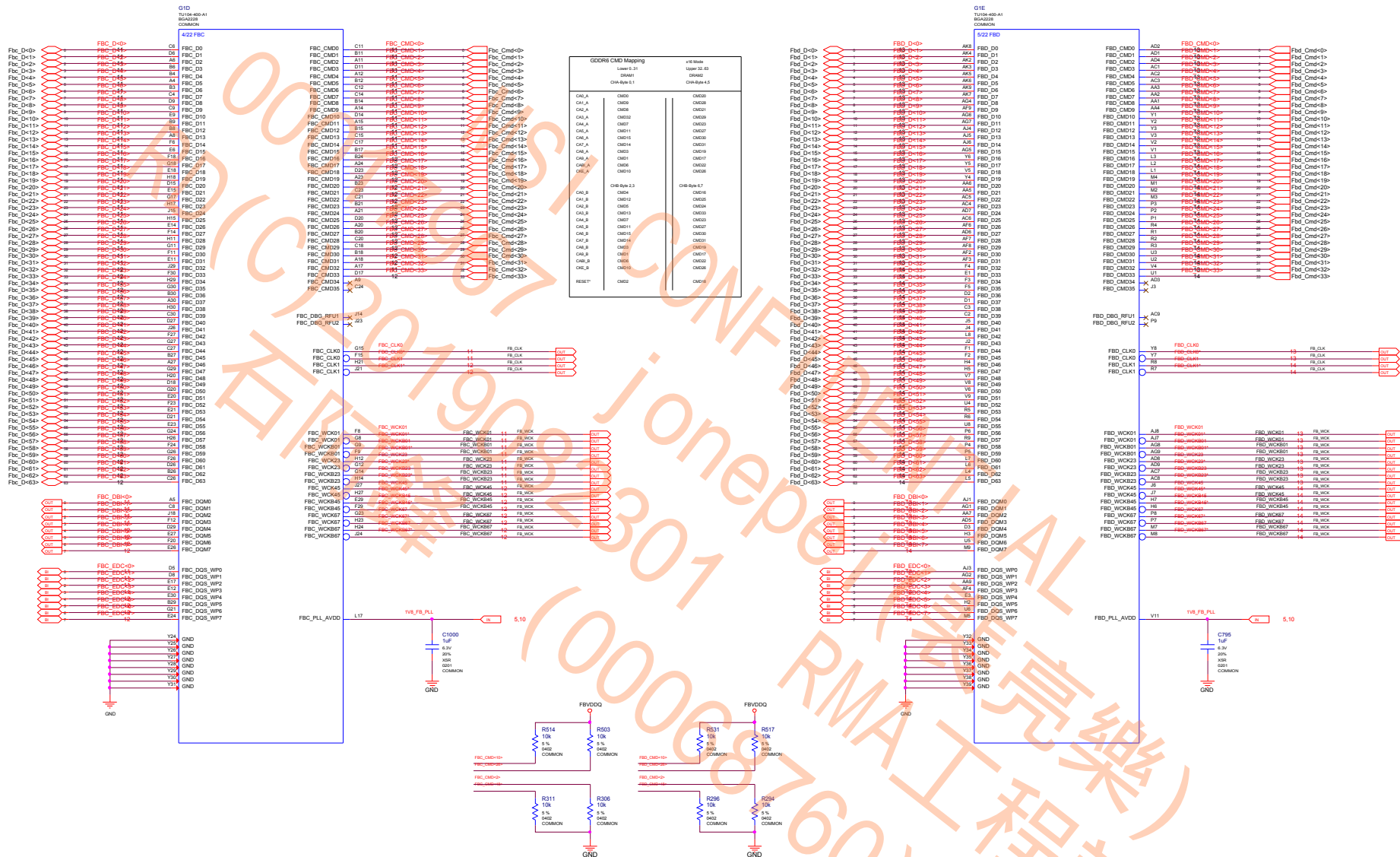


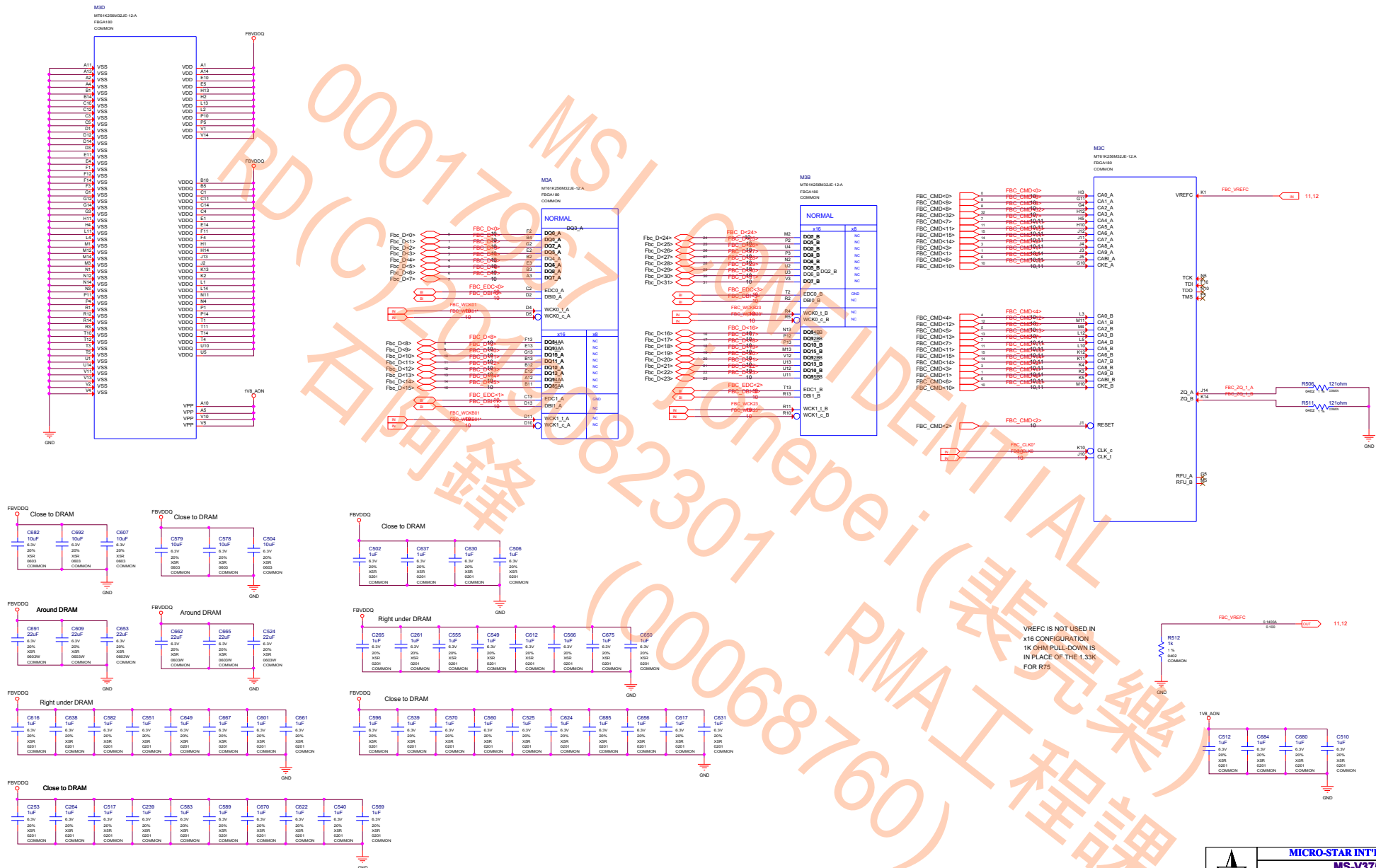


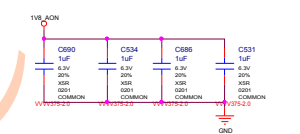
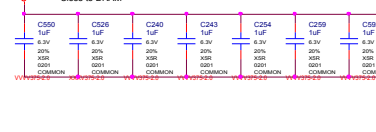
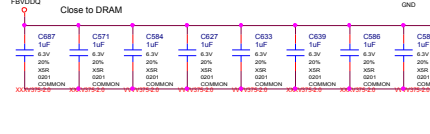
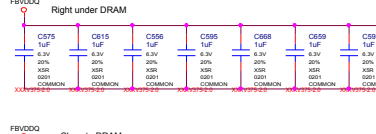
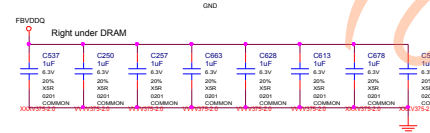
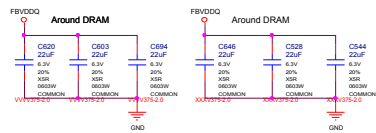
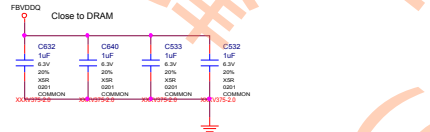
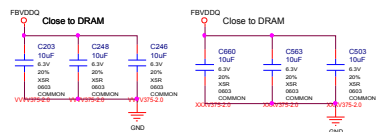
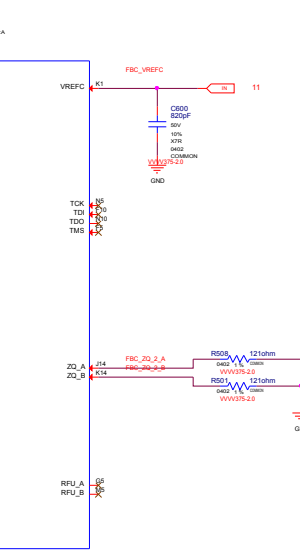
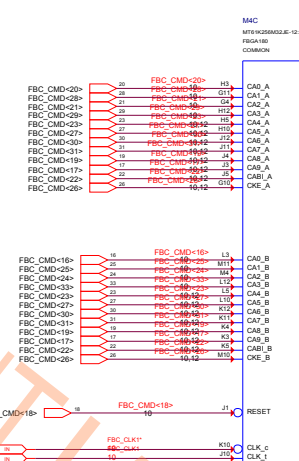
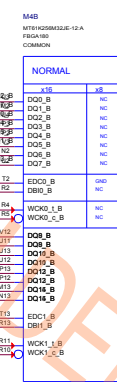
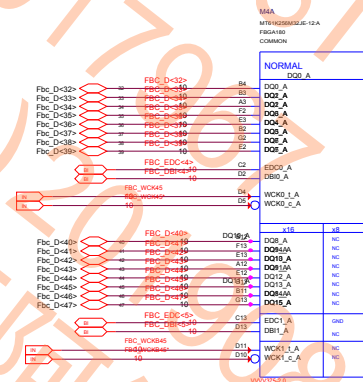
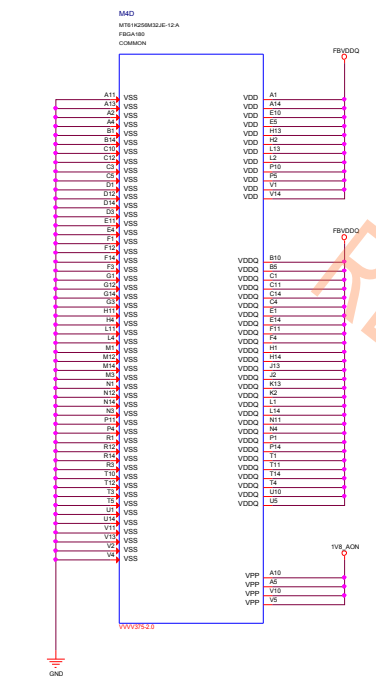
NO PEX GEN4 SUPPORT
DELETE RC TERMINATIONS

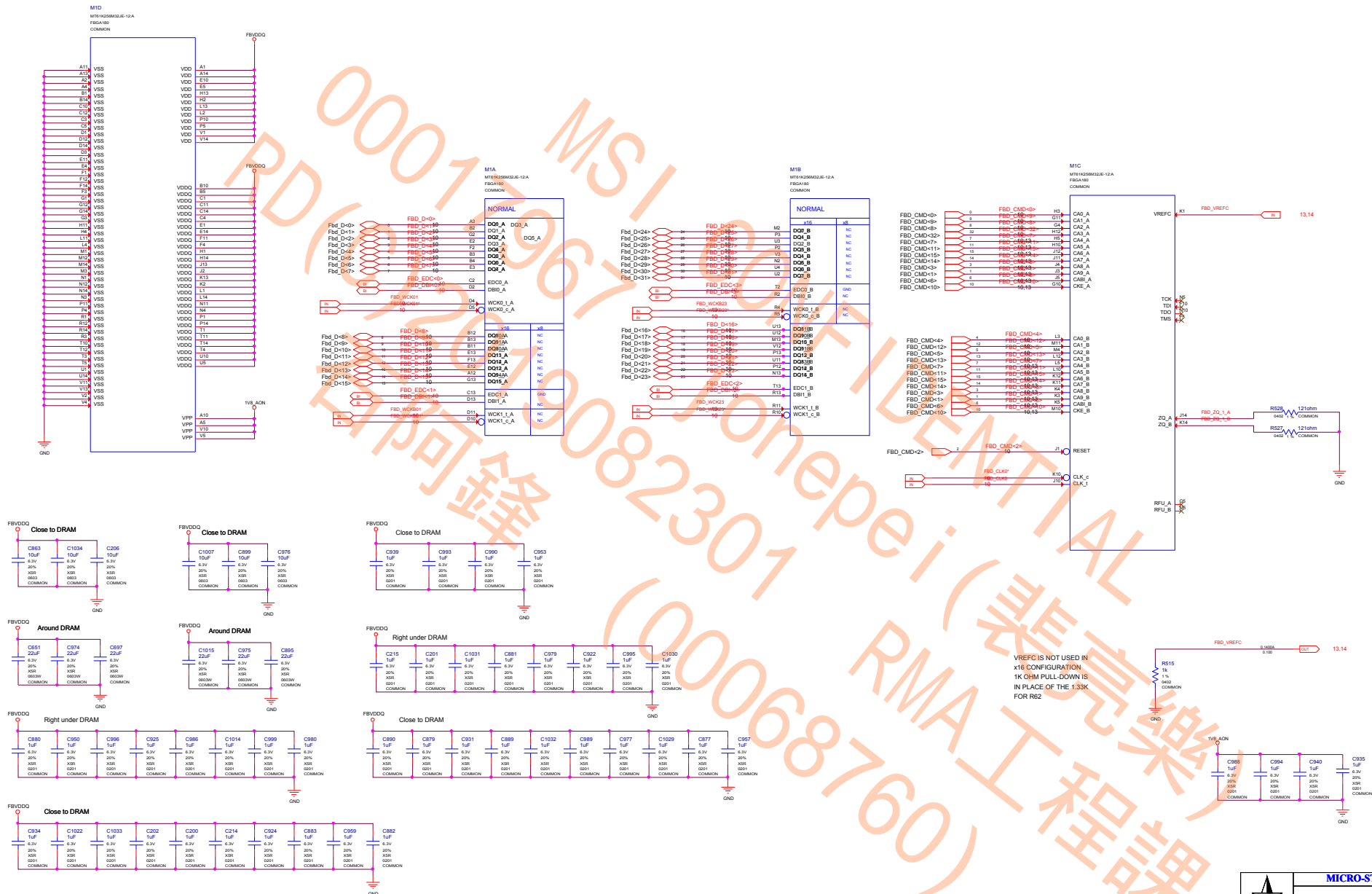


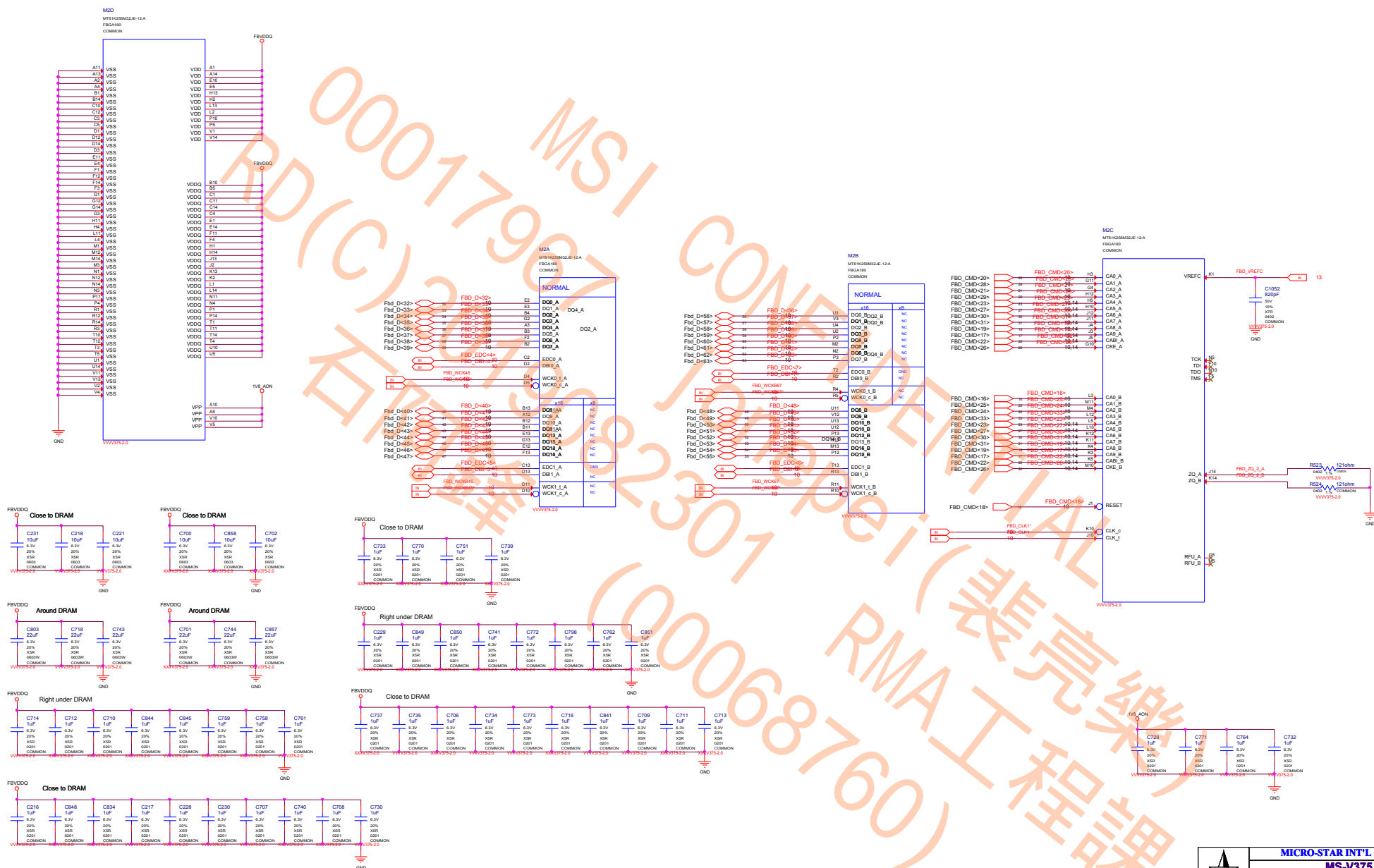


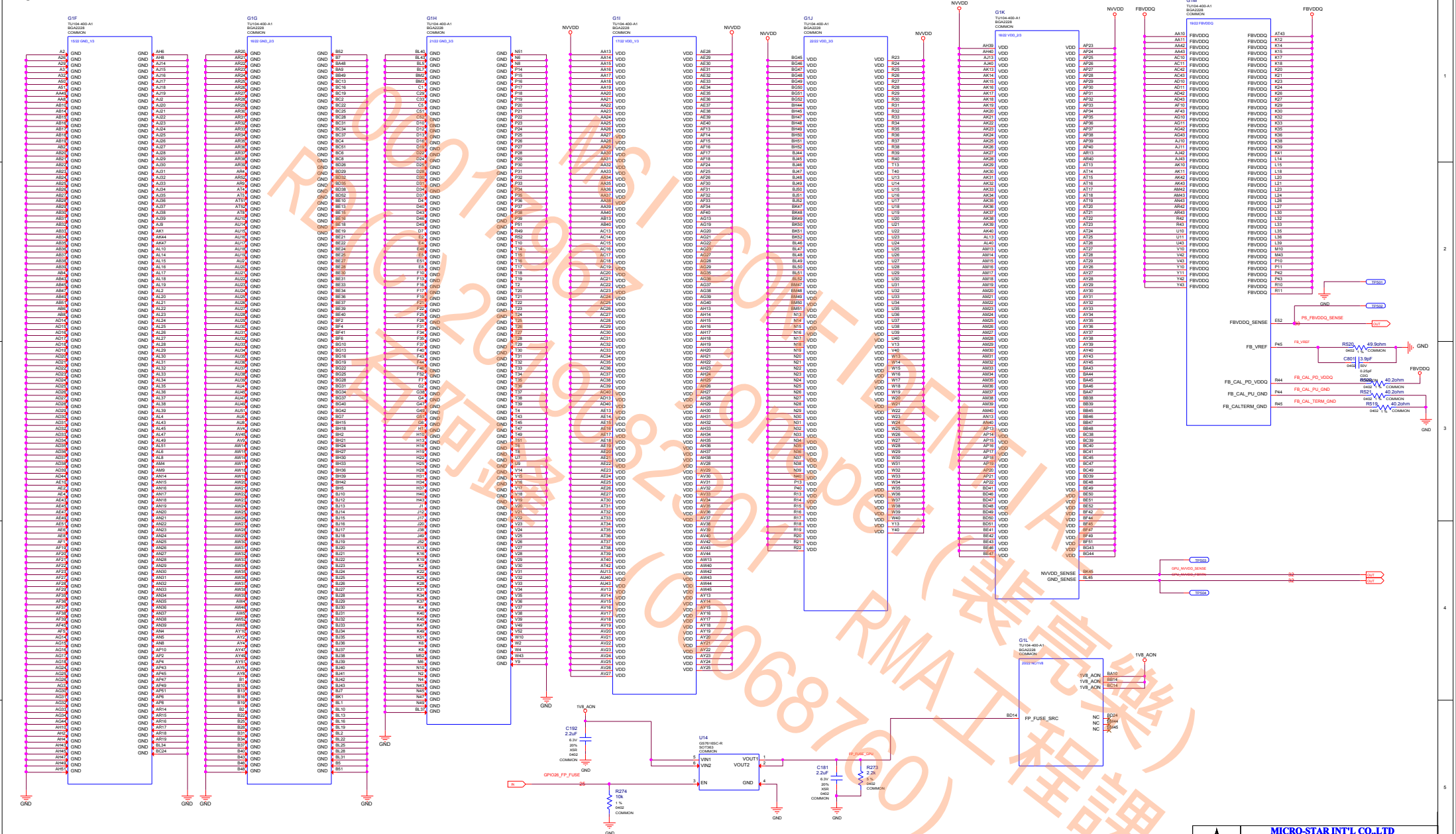








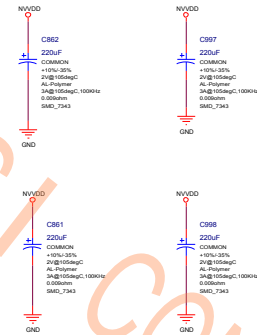




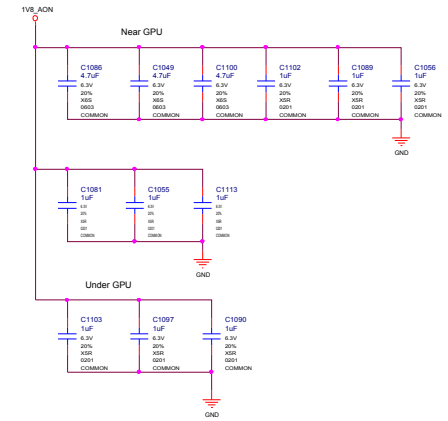
FBVDDQ



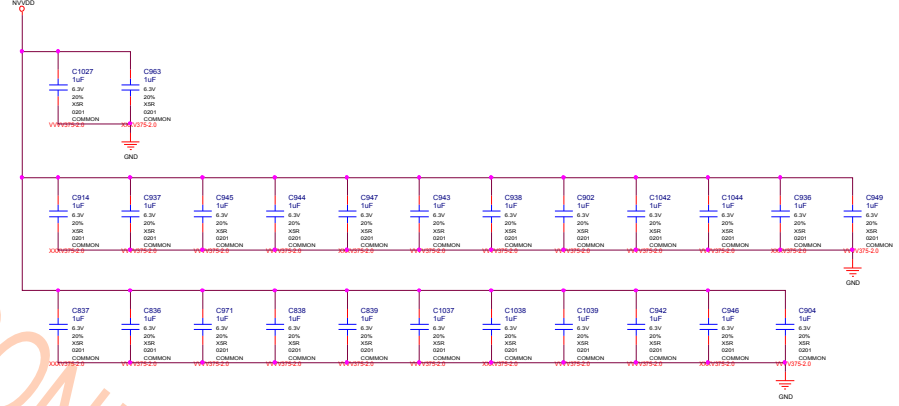
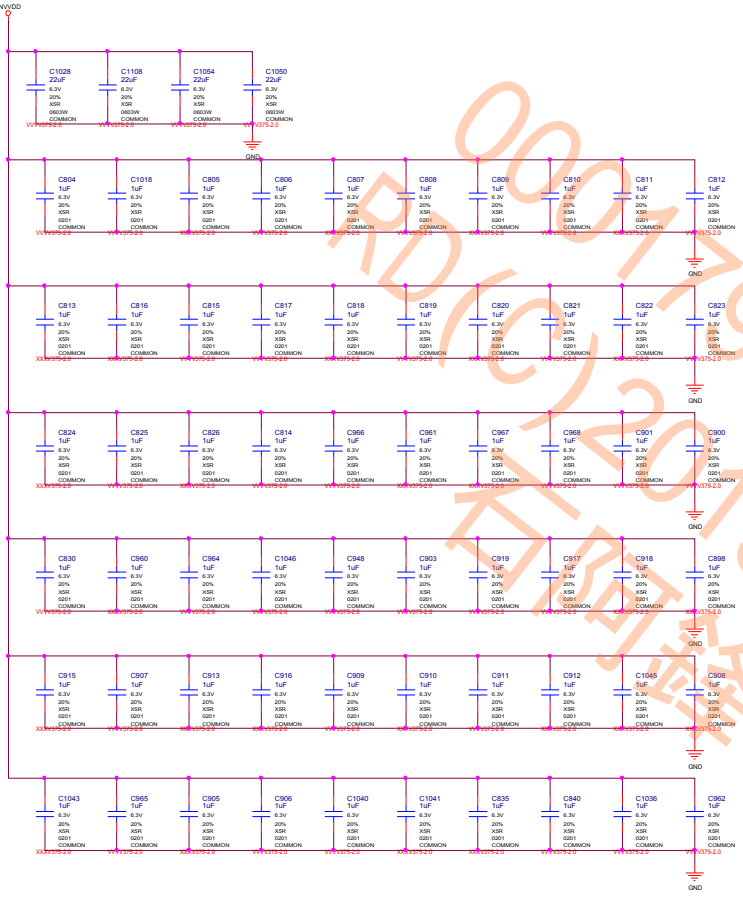
NVVDD



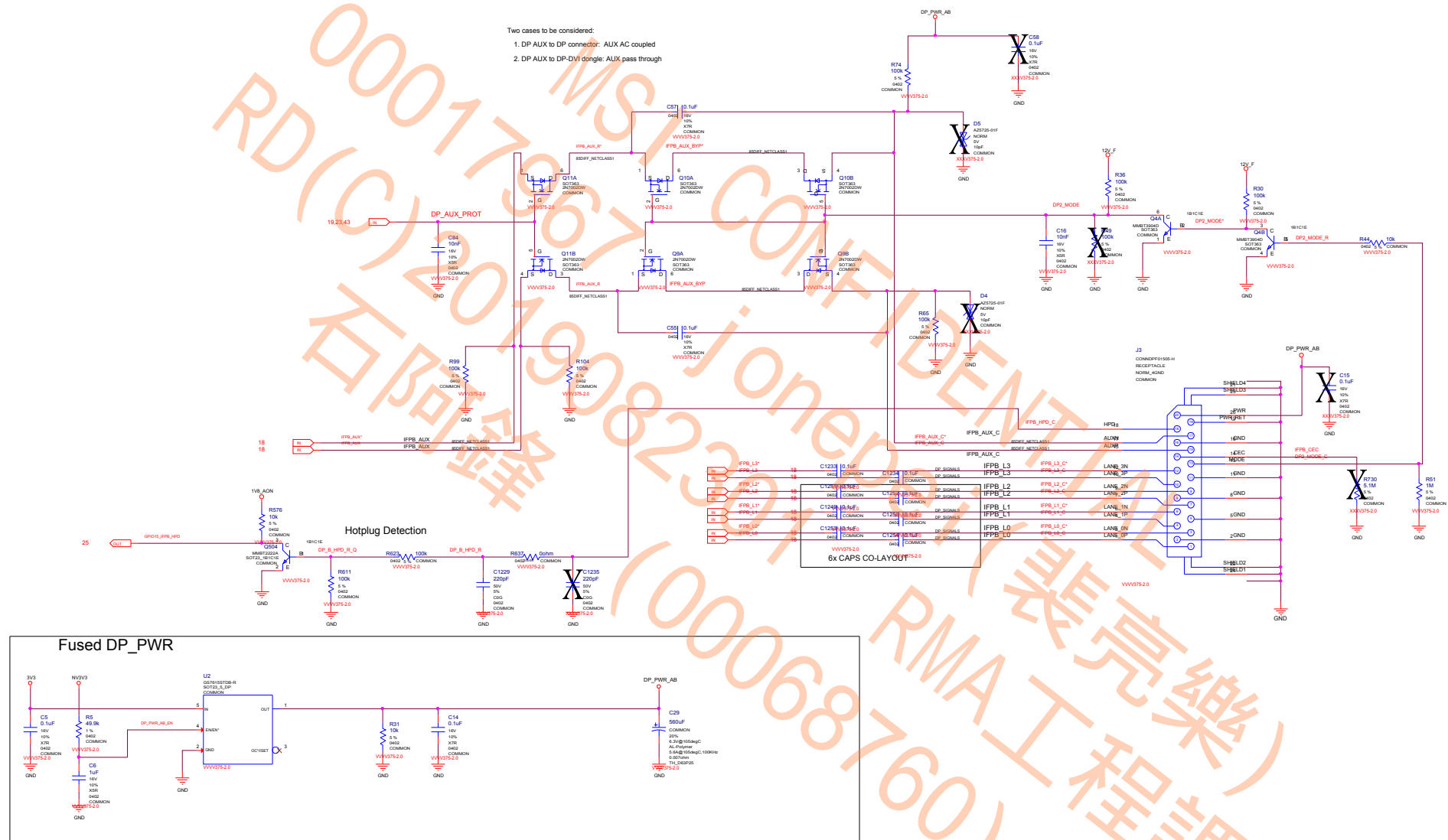
1V8_AON



NVDD



IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL

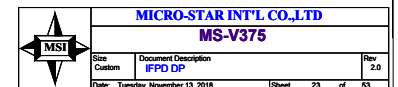
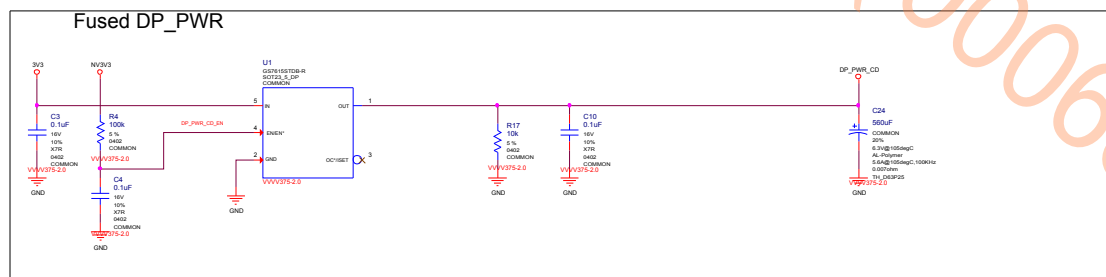
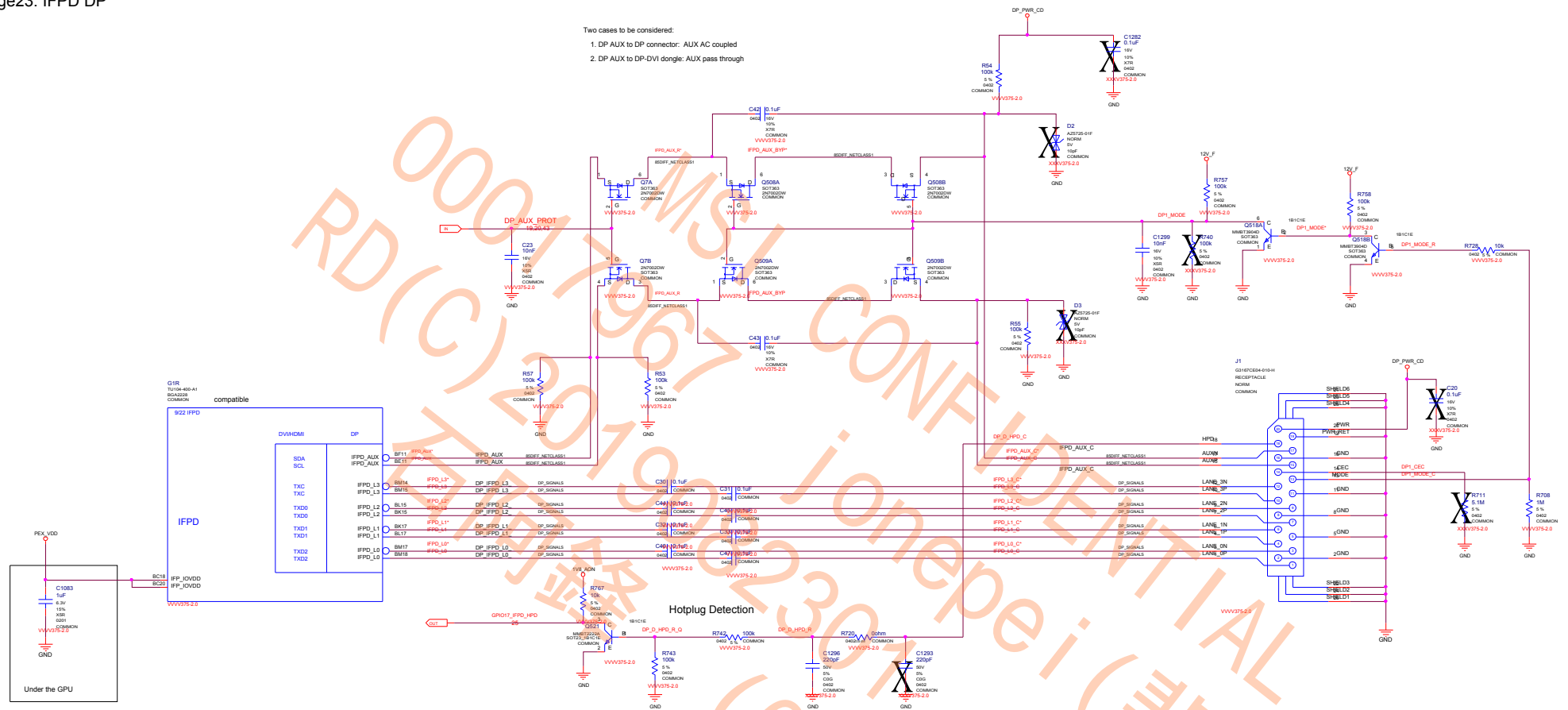


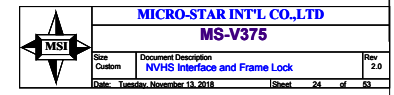
MICRO-STAR INT'L CO.,LTD
MS-V375

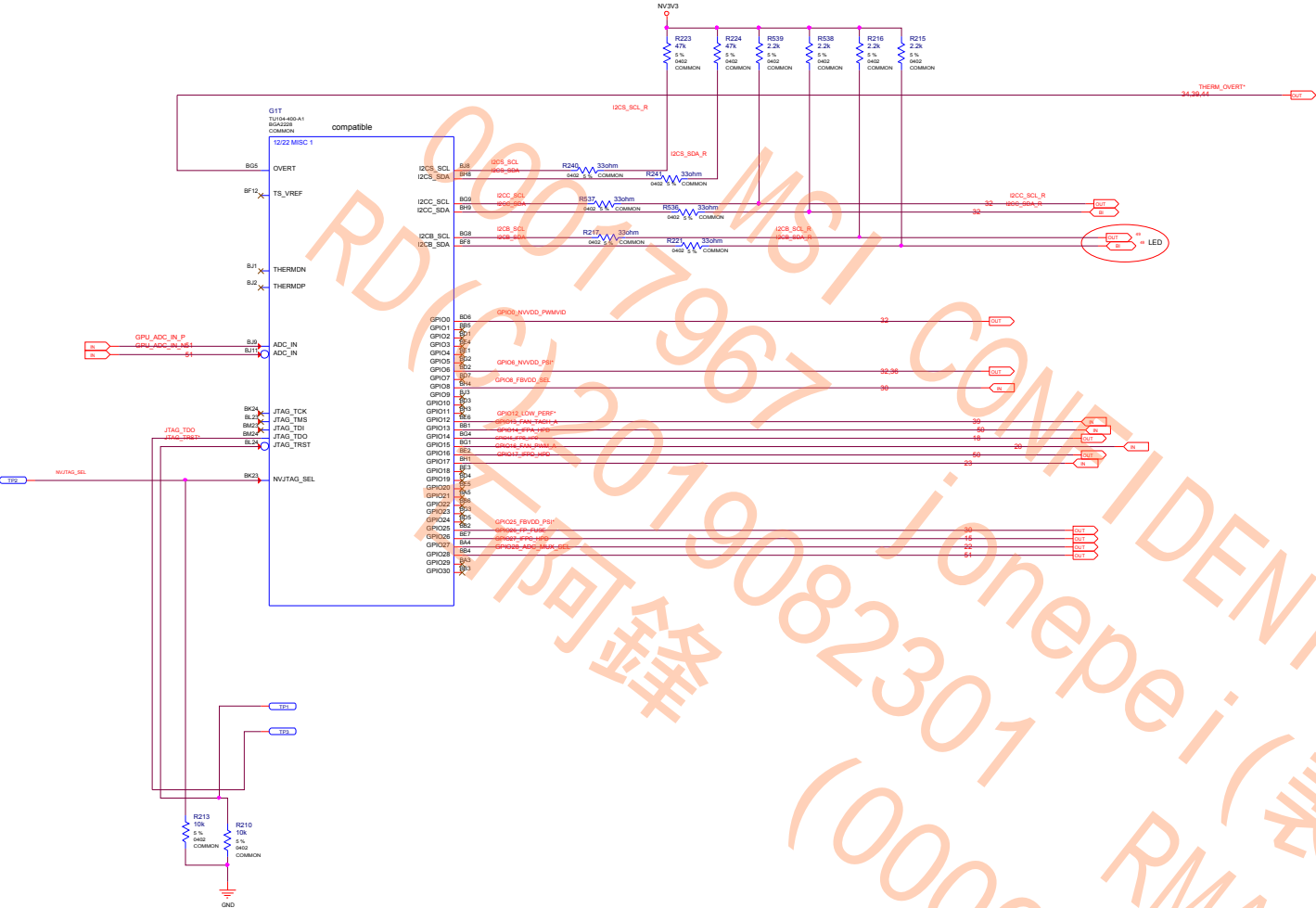
Size Custom	Document Description IFPB DP	Rev 2.0
Date: Tuesday, November 13, 2018		Sheet 20 of 53

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through







STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0].FS_OVERT	1.ENABLE 0.DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

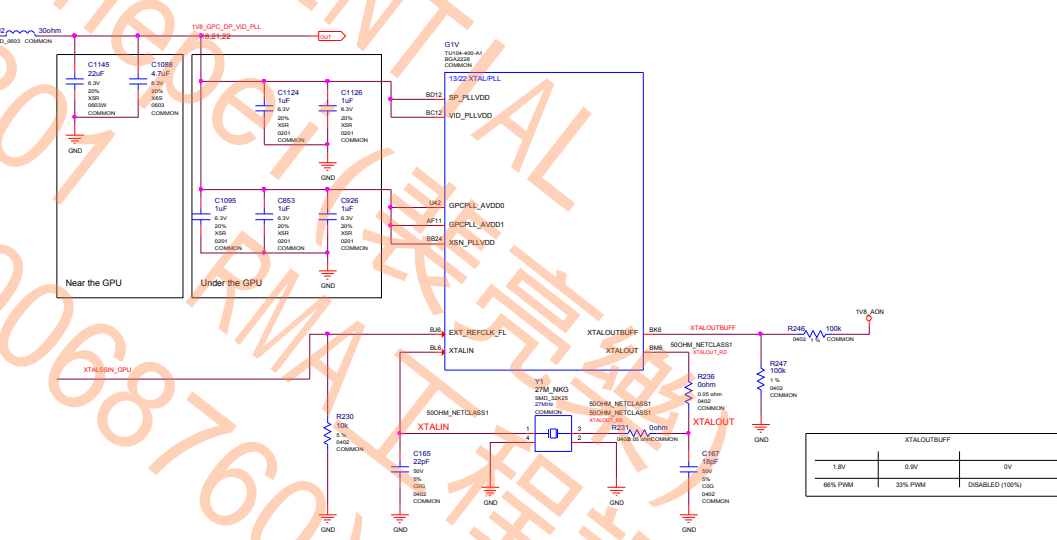
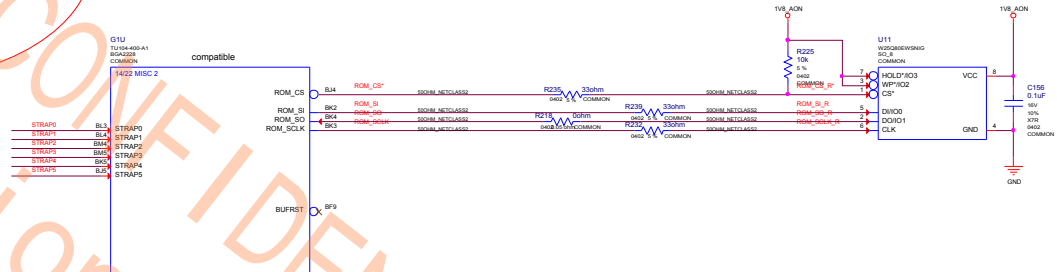
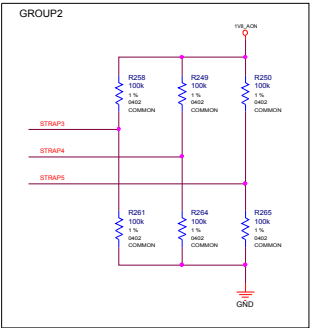
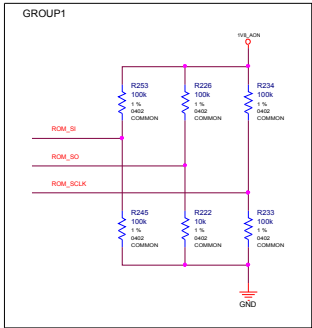
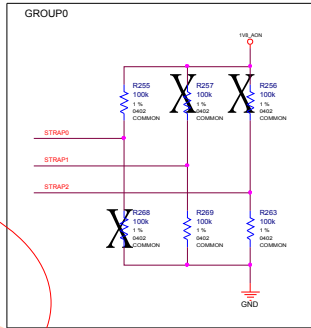
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

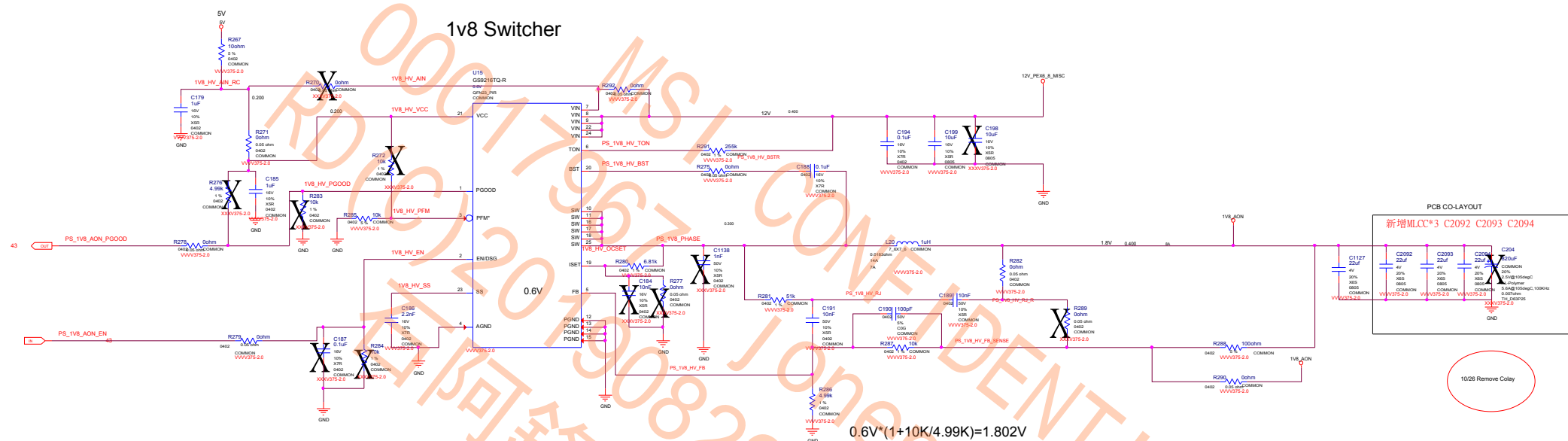
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

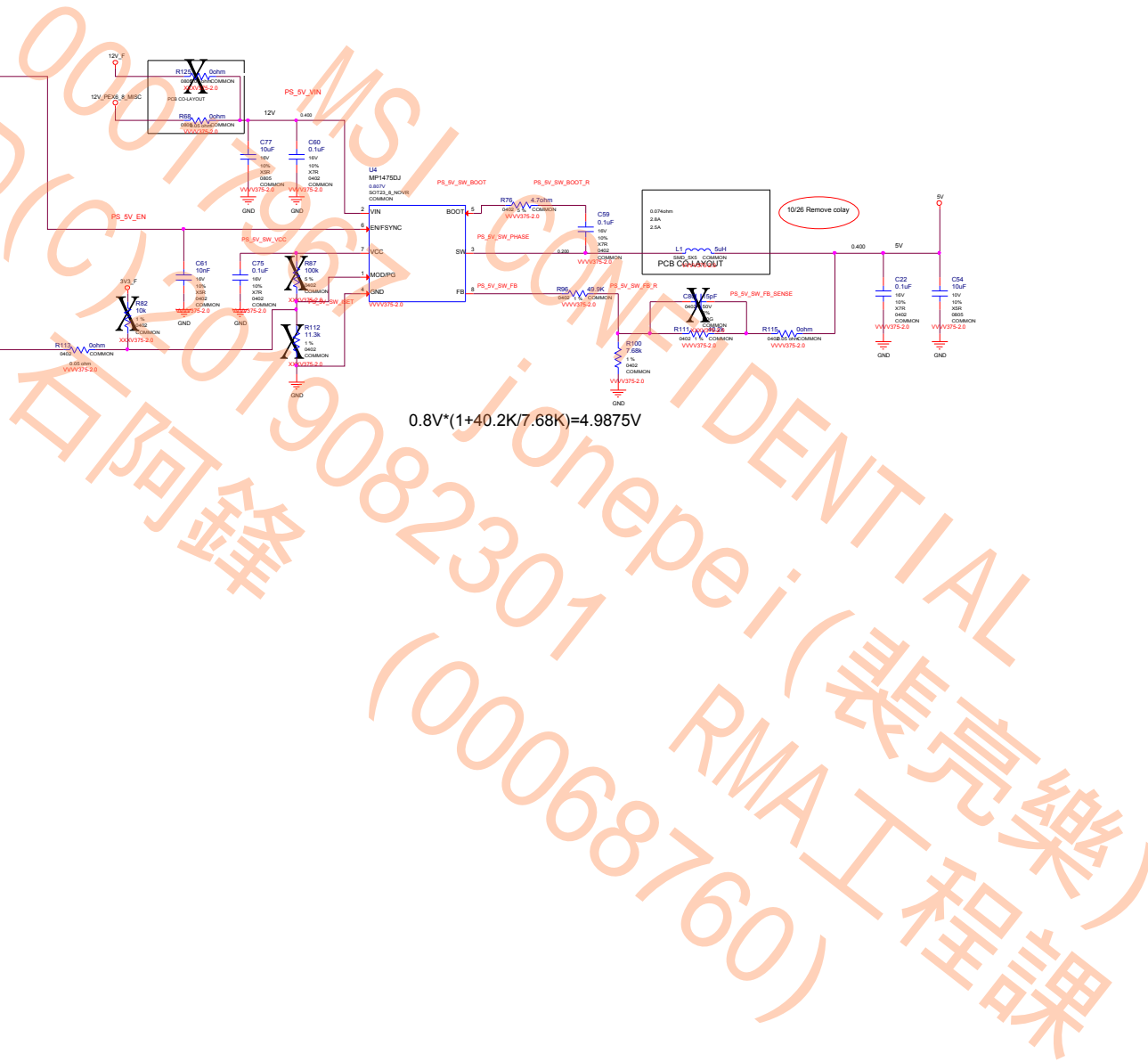
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

注意上件的MEM Straps



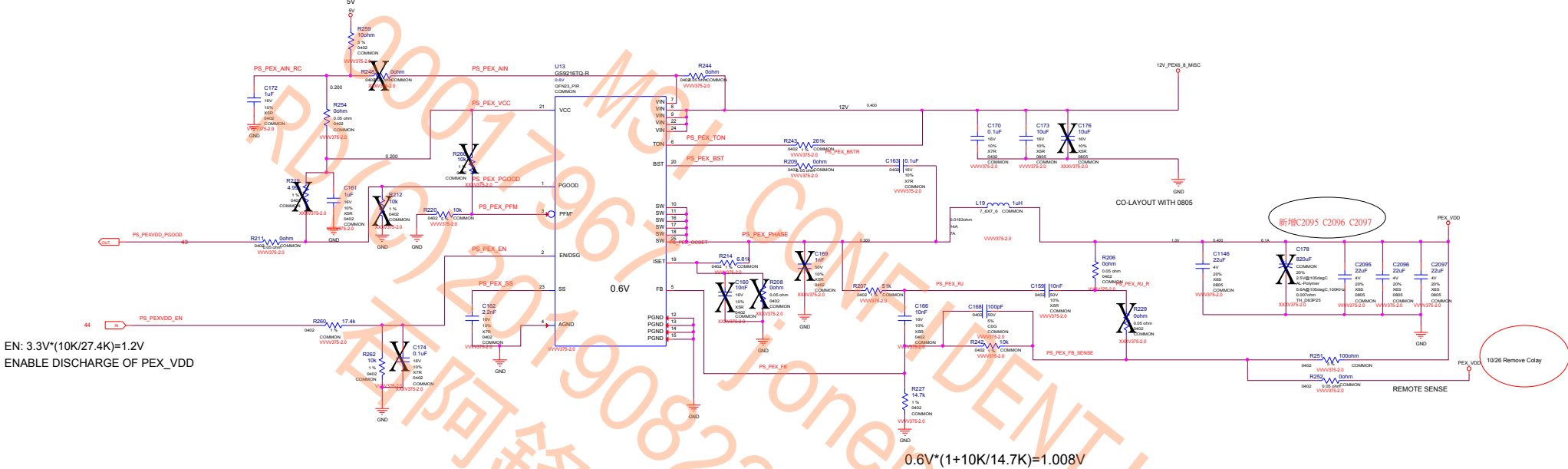
XTALOUTBUFF		
1.8V	0.9V	0V
66% PWM	33% PWM	DISABLED (100%)

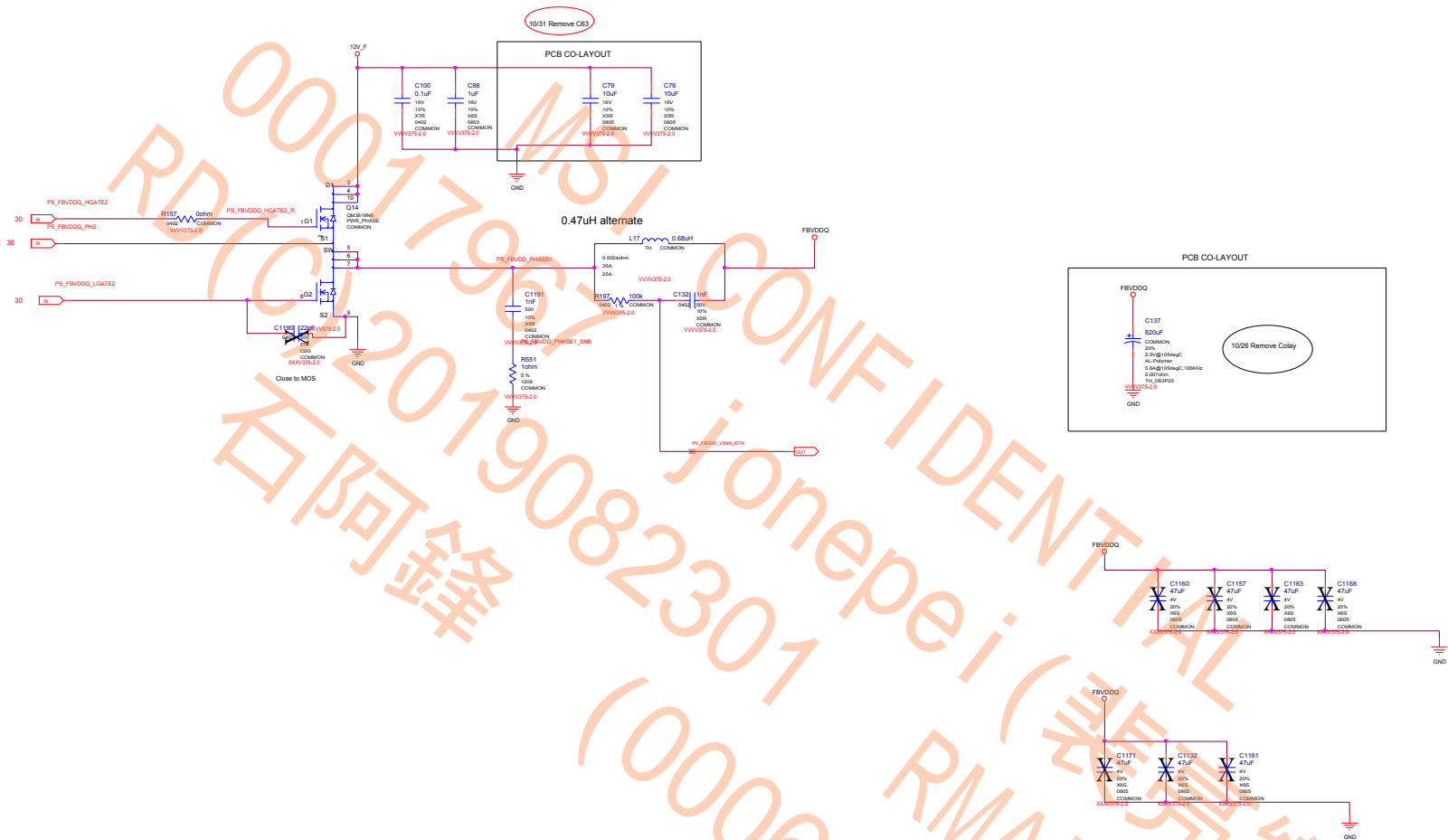


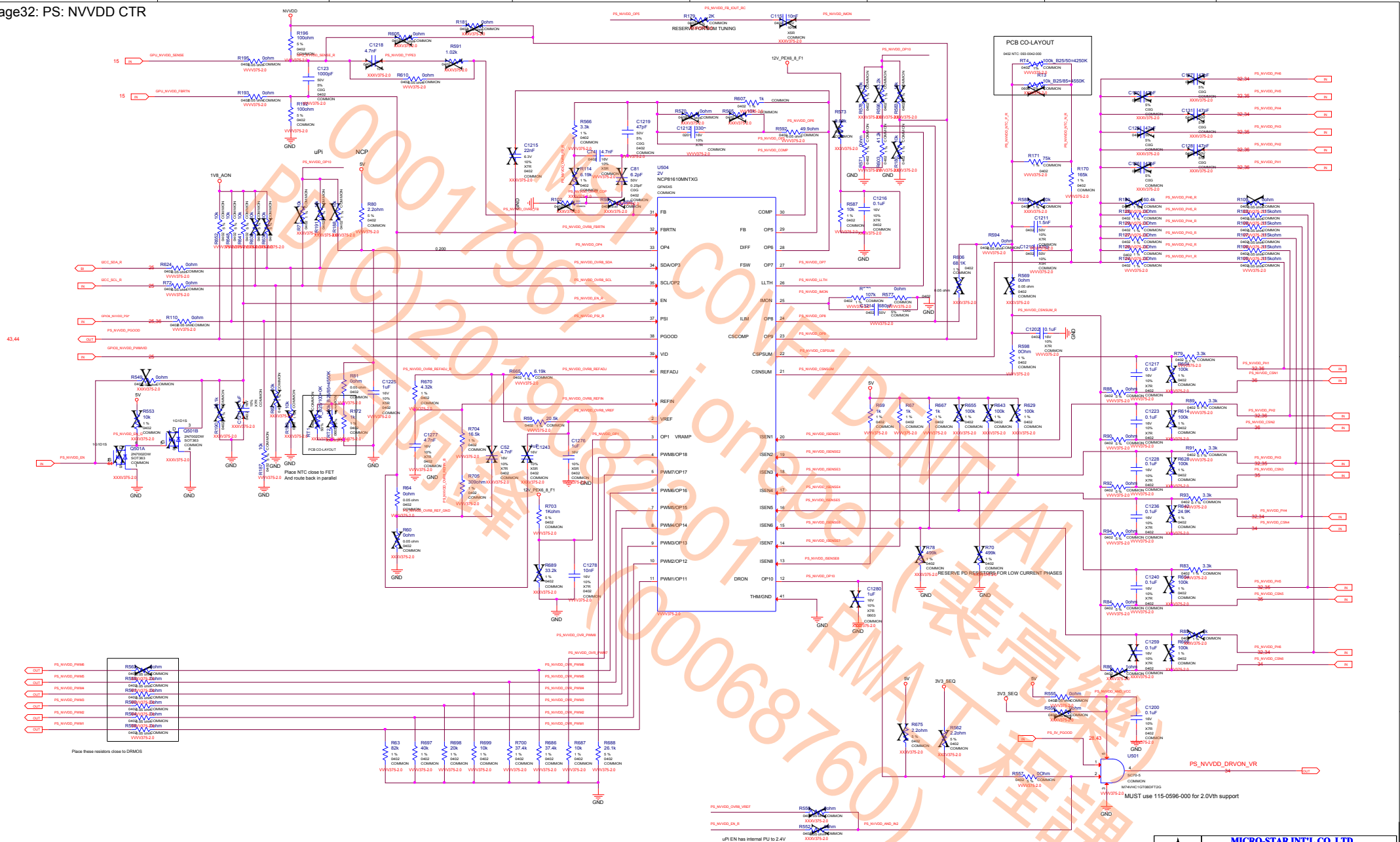


$$0.8V \cdot (1 + 40.2K / 7.68K) = 4.9875V$$

PEX Switcher

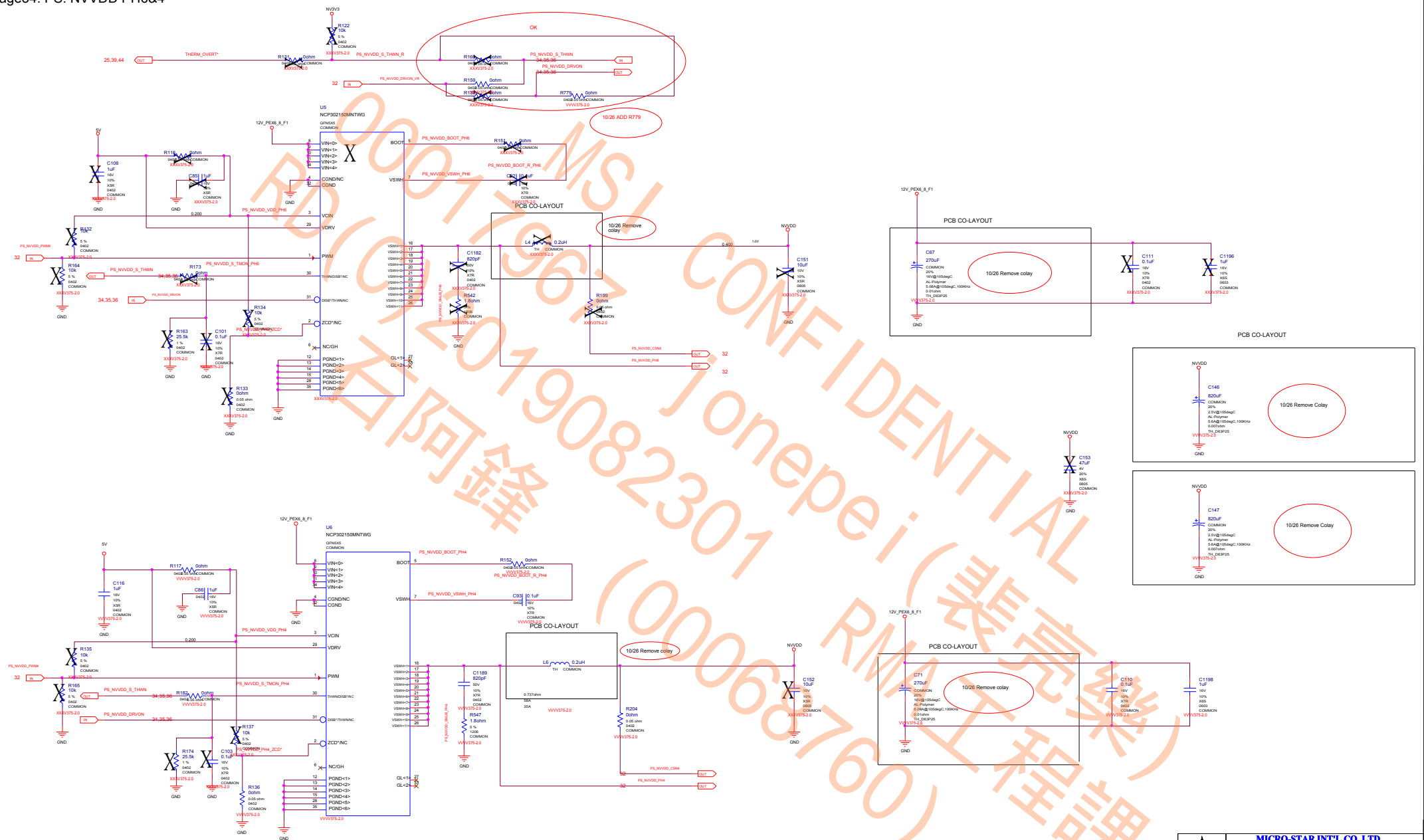


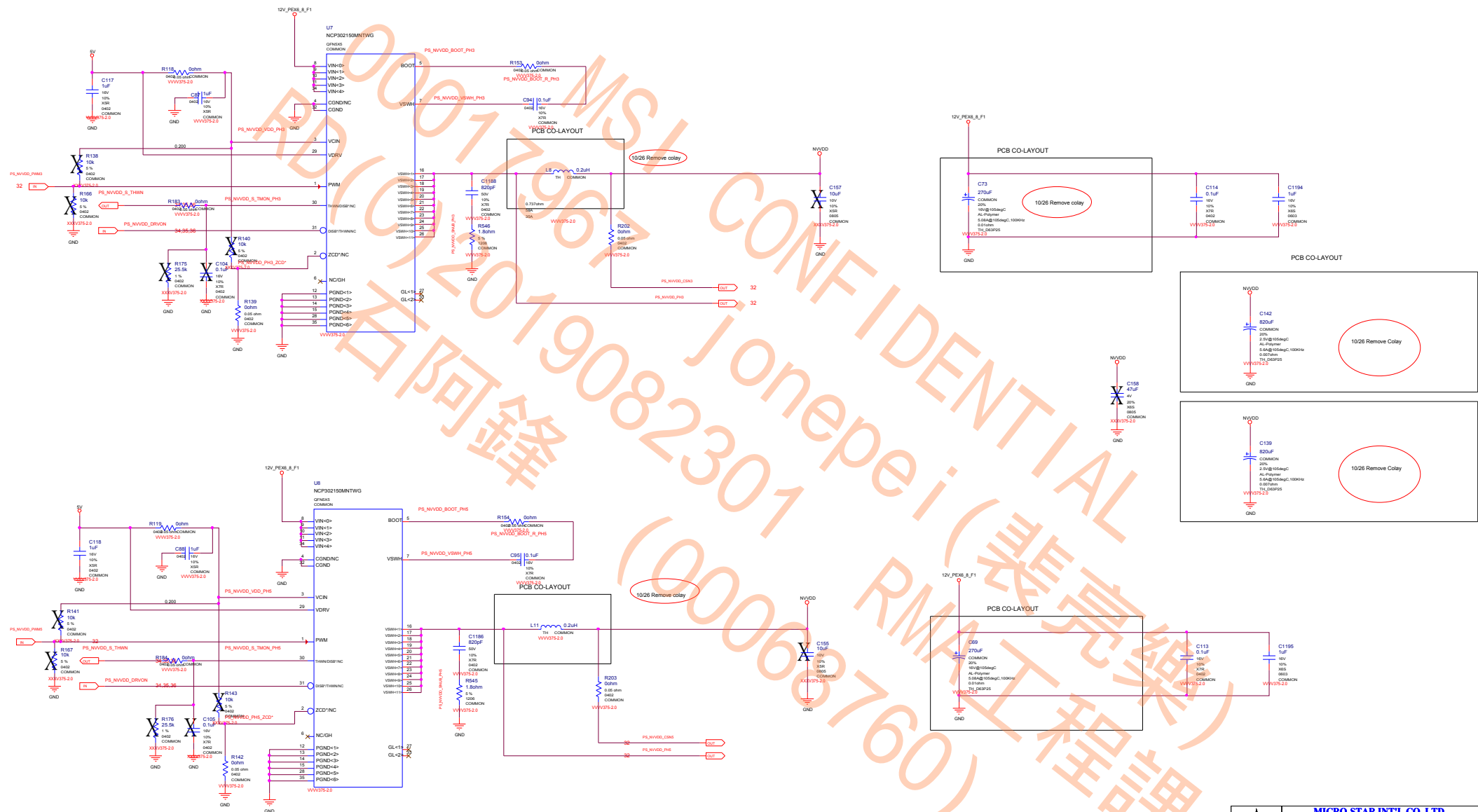


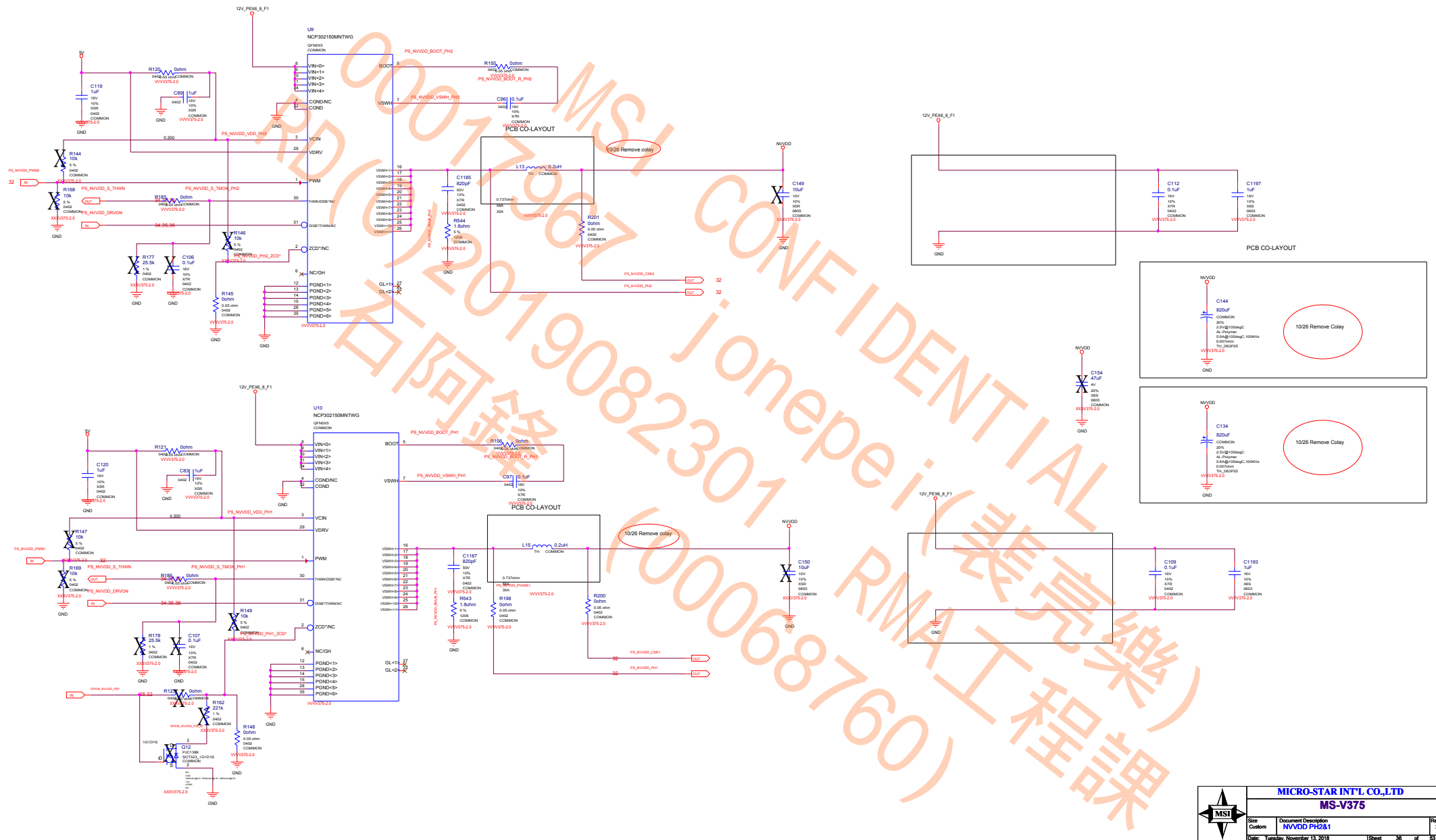


DROP OVR3i SOLUTION


	MICRO-STAR INT'L CO.,LTD		
	MS-V375		
	Size	Document Description	Rev
	Custom	PS: NVVDD CTR OVR3i	2.0
Date: Tuesday, November 13, 2018		Sheet 33 of 53	

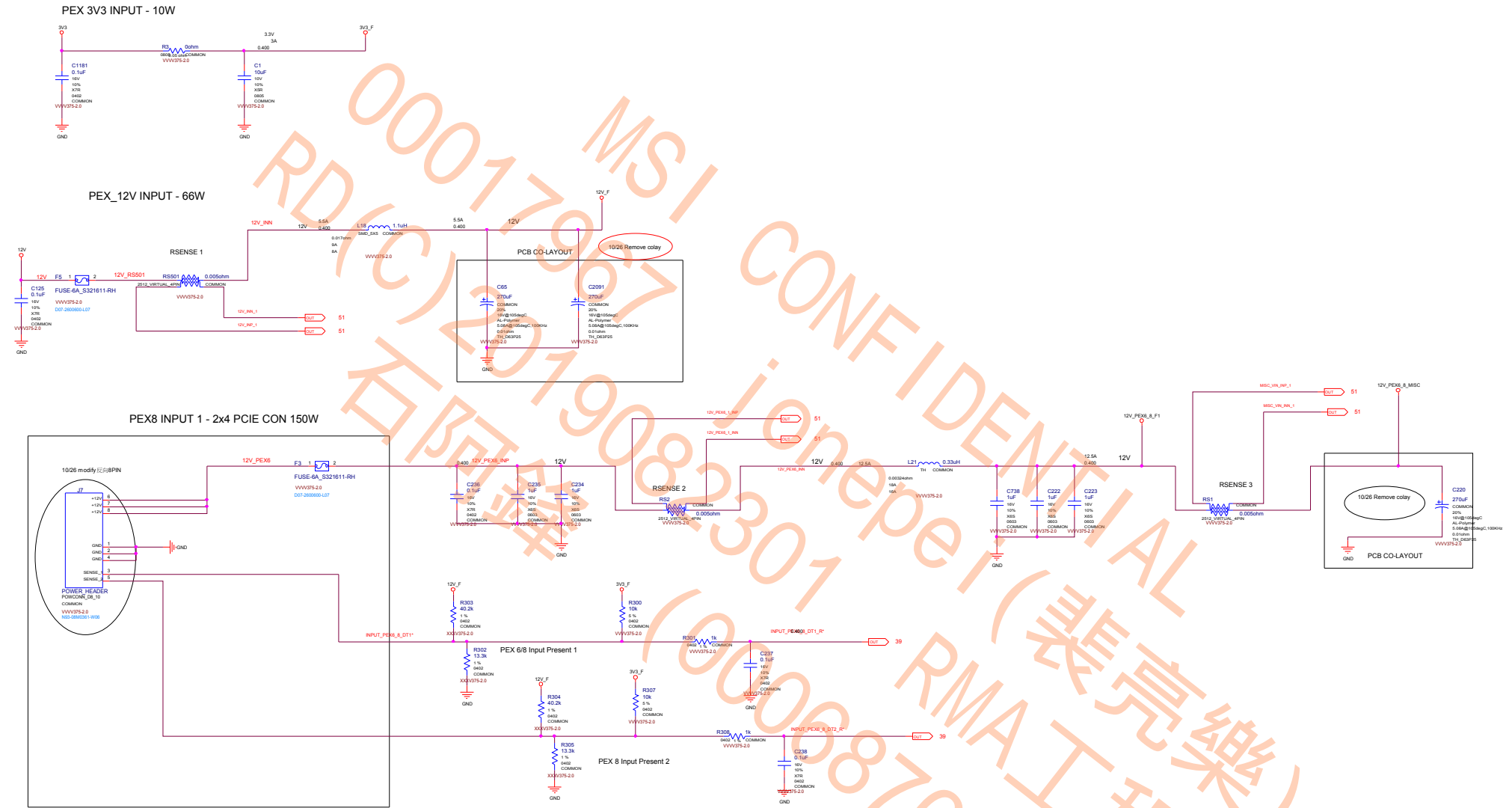


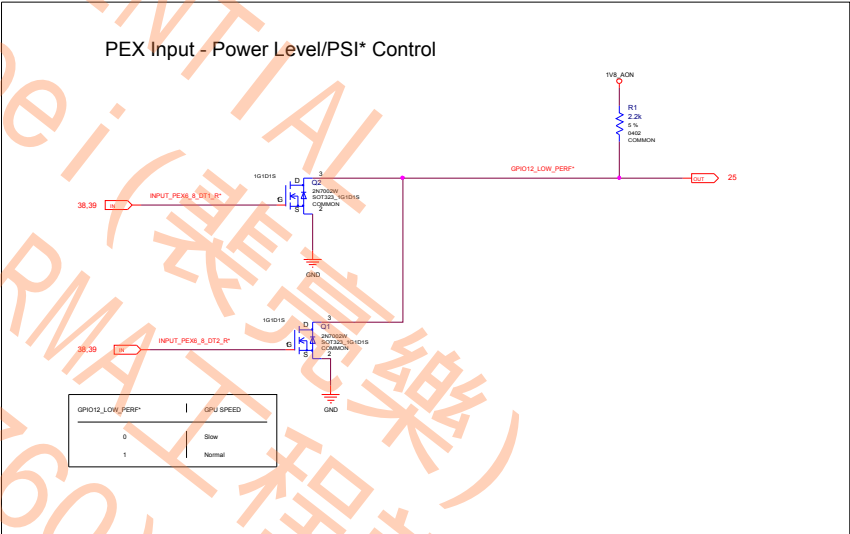
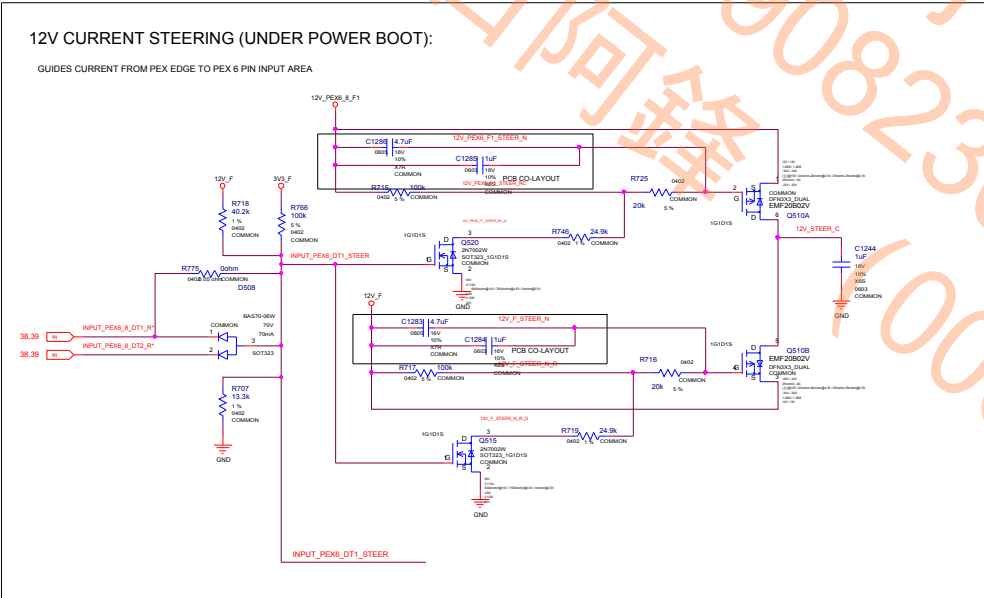
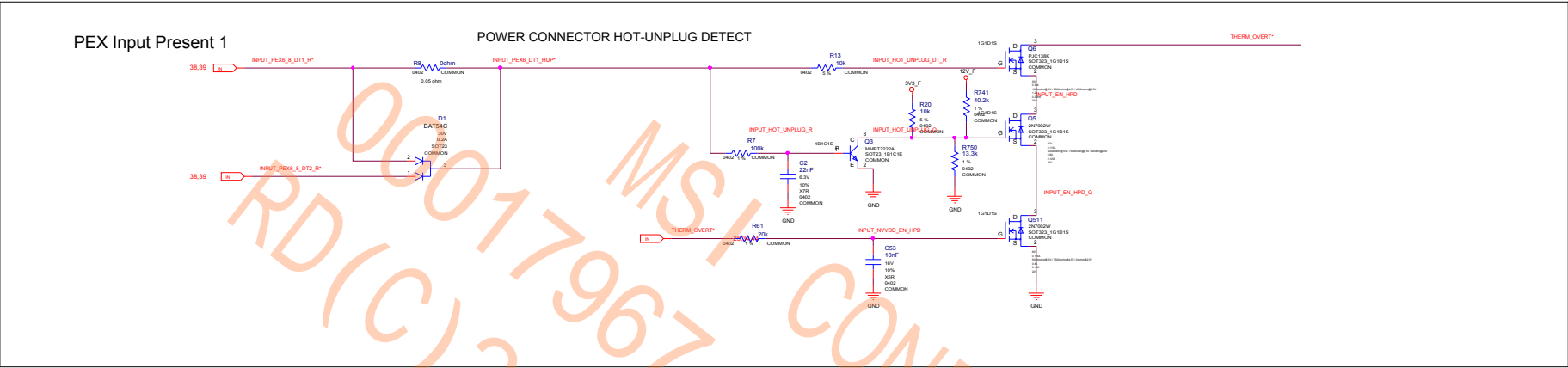




DELETE RAIL BALANCE CIRCUIT

	MICRO-STAR INT'L CO.,LTD		
	MS-V375		
	Size	Document Description	Rev
	Custom	Input Power Balancing Switcher	2.0
Date: Tuesday, November 13, 2018		Sheet	37 of 53





MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2019082301 RMA工程課
石阿鋒 (00068760)

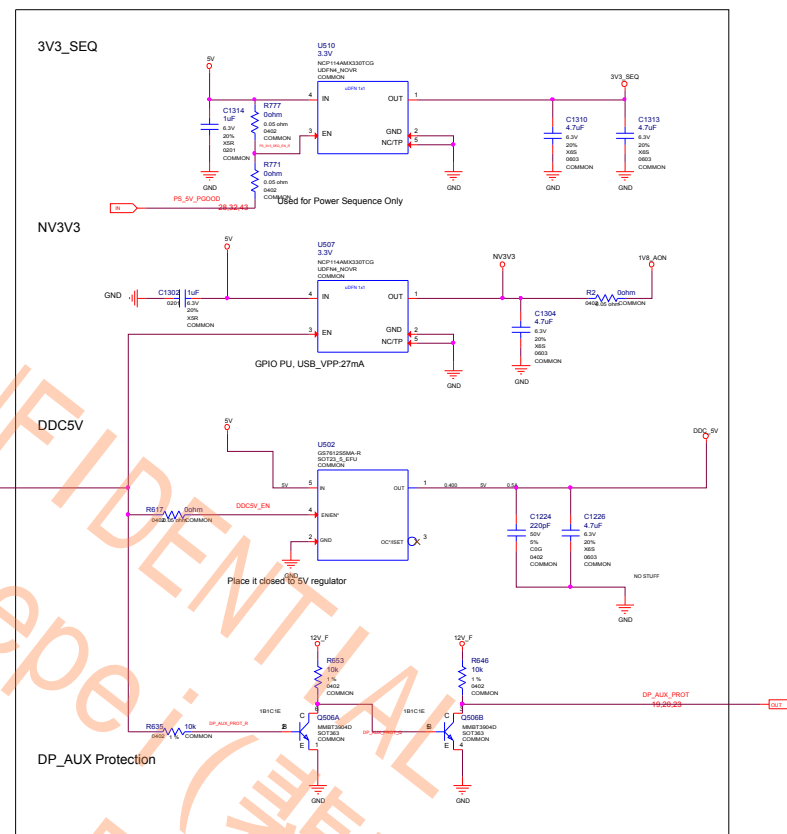
	MICRO-STAR INT'L CO.,LTD		
	MS-V375		
	Size	Document Description	Rev
	Custom	BUCKBOOST	2.0
Date: Tuesday, November 13, 2018		Sheet 40 of 53	

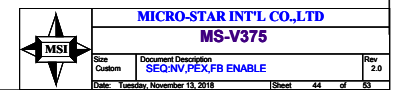
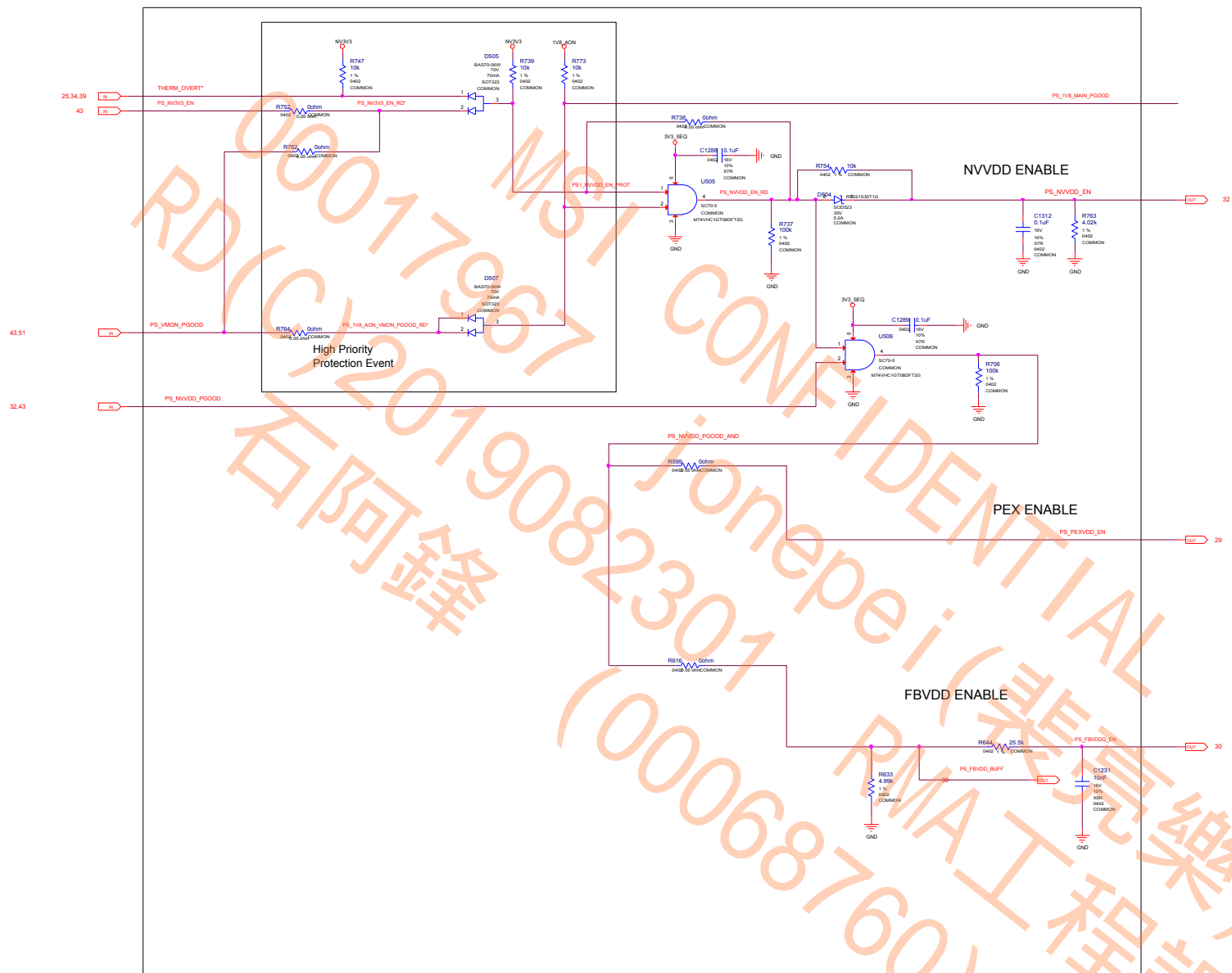
MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2019082301 RMA工程課
石阿鋒 (00068760)

	MICRO-STAR INT'L CO.,LTD	
	MS-V375	
	Size Custom	Document Description PPC
	Date: Tuesday, November 13, 2018	Rev 2.0
		Sheet 41 of 53

MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2019082301 RMA工程課
石阿鋒 (00068760)

MICRO-STAR INT'L CO.,LTD		
MS-V375		
Size	Document Description	Rev
Custom	12V & 3V3_A SWITCHER	2.0
Date: Tuesday, November 13, 2018		Sheet 42 of 53




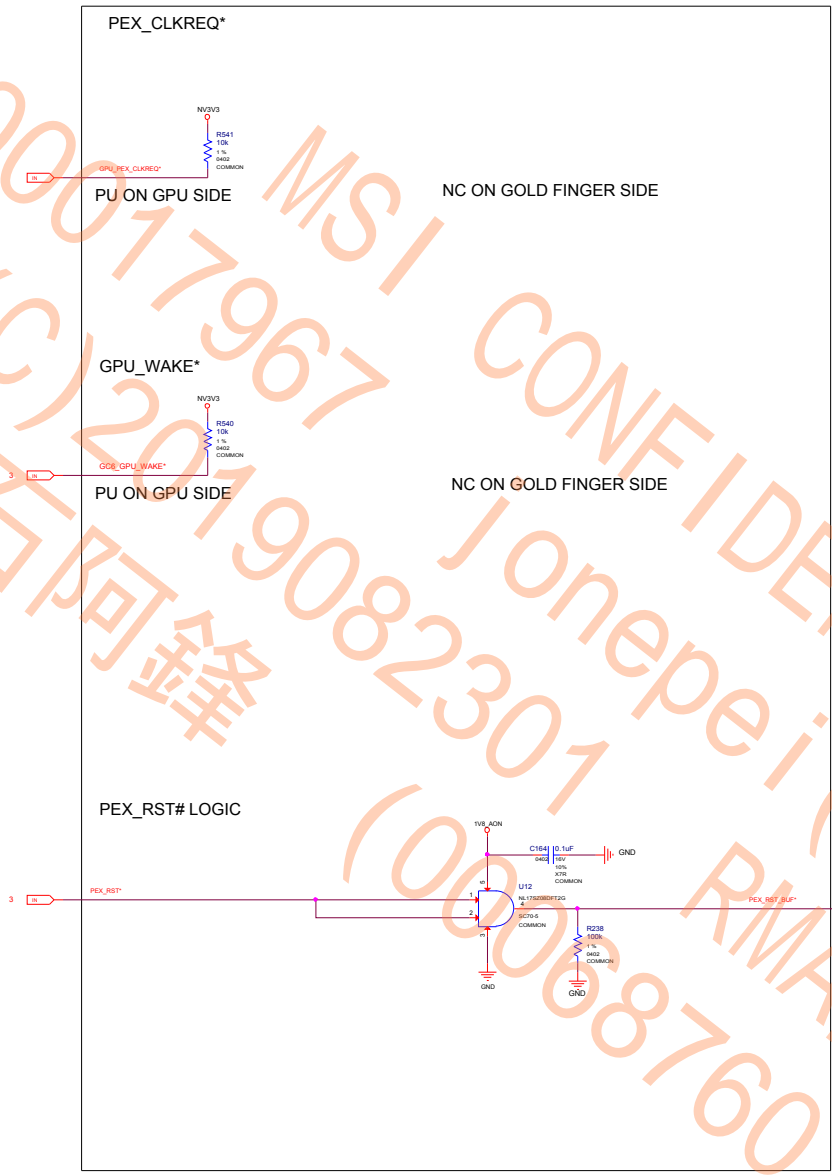


MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2019082301 RMA工程課
石阿鋒 (00068760)

MICRO-STAR INT'L CO.,LTD		
MS-V375		
Size	Document Description	Rev
Custom	SEQUENCE:Voltage Monitor	2.0
Date: Tuesday, November 13, 2018		Sheet 45 of 53

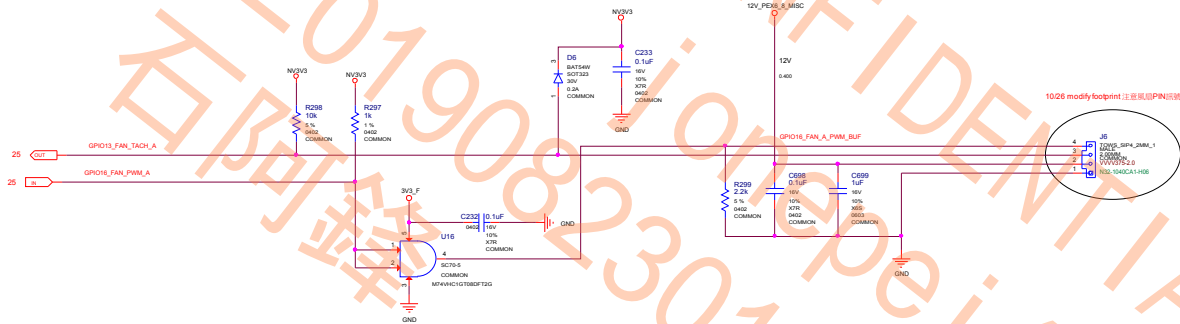
MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2019082301 RMA工程課
石阿鋒 (00068760)

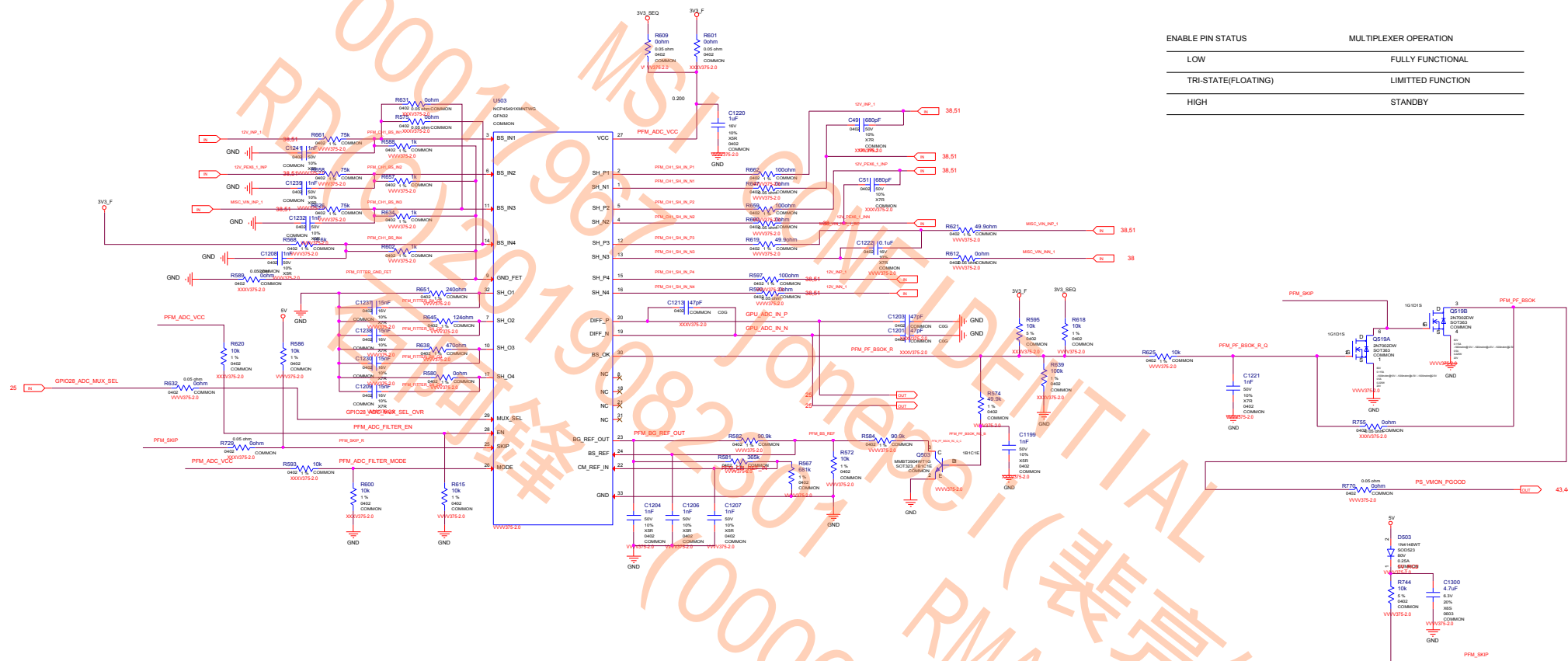
	MICRO-STAR INT'L CO.,LTD		
	MS-V375		
	Size	Document Description	Rev
	Custom	SEQUENCE:Discharge	2.0
Date: Tuesday, November 13, 2018		Sheet 46 of 53	



MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2019082301 RMA工程課
石阿鋒 (00068760)

		MICRO-STAR INT'L CO.,LTD	
		MS-V375	
Size	Document Description	Rev	
Custom	LOGO LED	2.0	
Date: Tuesday, November 13, 2018		Sheet	48 of 53

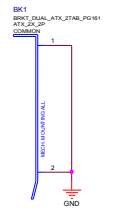




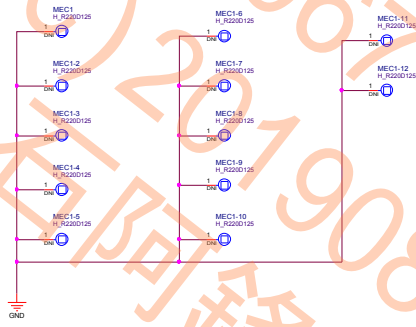
MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

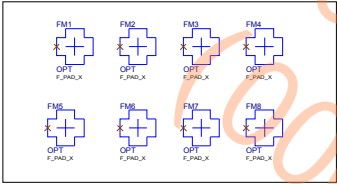
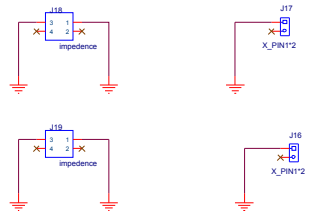
Bracket:




MOUNTING HOLES FOR HS:



BACK STIFFENER:



MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2019082301 RMA工程課
石阿鋒 (00068760)

	MICRO-STAR INT'L CO.,LTD	
	MS-V375	
	Size Custom	Document Description PTC
	Date: Tuesday, November 13, 2018	Rev 2.0
Sheet 53 of 53		